$$B1_{M_N} = 4^N B1_{M_N} - \sum_{n=0}^{N-1} 4^n$$

$$B2_{M_N} = \sum_{n=0}^{N} 4^n$$

; and

in a fourth row a third break point B3 of a third incrementation sequence is determined by the relationship

$$B3_{M_N} = 2 \times 4^N + 2$$

wherein M_N represents the memory of an Nth stage of said FFT processor.

8. The receiver according to claim 1, further comprising channel estimation and correction circuitry comprising:

pilot location circuitry receiving a transformed digital signal representing a frame from said FFT processor for locating pilot carriers therein, wherein said pilot carriers are spaced apart in a carrier spectrum of said transformed digital signal at intervals K and have predetermined magnitudes, said pilot location circuitry comprising:

a first circuit for computing an order of carriers in said transformed digital signal modulo K;

K accumulators coupled to said second circuit for accumulating magnitudes of said carriers in said transformed digital signal, said accumulated magnitudes defining a set; and

a correlation circuit for correlating K sets of accumulated magnitude values with said predetermined magnitudes, wherein a first member having a position calculated modulo K in each of said K sets is uniquely offset from a start position of said frame.

9. The receiver according to claim 8, wherein said pilot location circuitry further comprises a bit reversal circuit for reversing a bit order of said transformed digital signal.

10. The receiver according to claim 7, wherein said magnitudes of said carriers and said predetermined magnitudes are amplitudes.

11. The receiver according to claim 7, wherein said magnitudes of said carriers and said predetermined magnitudes are absolute values.

12. The receiver according to claim 7, wherein said correlation circuitry further comprises a peak tracking circuit for determining a spacing between a first peak and a second peak of said K sets of accumulated magnitudes.

13. The receiver according to claim 7, wherein said channel estimation and correction circuitry further comprises:

an interpolating filter for estimating a channel response between said pilot carriers; and

a multiplication circuit for multiplying data carriers output by said FFT processor with a correction coefficient produced by said interpolating filter.

14. The receiver according to claim 7, wherein said channel estimation and correction circuitry further comprises

a phase extraction circuit accepting a data stream of phase-uncorrected I and Q data from said FFT processor, and producing a signal representative of a phase angle of said uncorrected data, said phase extraction circuit including an accumulator for accumulating the phase angles of succeeding phase-uncorrected I and Q data.

15. The receiver according to claim 14, said channel estimation and correction circuitry further comprises:

an automatic frequency control circuit coupled to said phase extraction circuit and said accumulator, comprising;

a memory for storing an accumulated common phase error of a first symbol carried in said phase-uncorrected I and Q data;

wherein said accumulator is coupled to said memory and accumulates a difference between a common phase error of a plurality of pilot carriers in a second symbol and a common phase error of corresponding pilot carriers in said first symbol;

an output of said accumulator being coupled to said I/Q demodulator.

16. The receiver according to claim 15, wherein said coupled output of said accumulator is enabled in said I/Q demodulator only during reception of a guard interval therein.

17. The receiver according to claim 14, said channel estimation and correction circuitry further comprises an automatic sampling rate control circuit coupled to said phase extraction circuit, comprising:

a memory for storing accumulated phase errors of pilot carriers in a first symbol carried in said phase-uncorrected I and Q data;

wherein said accumulator is coupled to said memory and accumulates differences between phase errors of pilot carriers in a second symbol and phase errors of corresponding pilot carriers in said first symbol to define a plurality of accumulated intersymbol carrier phase error differentials, a phase slope being defined by a difference between a first accumulated intersymbol carrier phase differential and a second accumulated intersymbol carrier phase differential;

an output of said accumulator being coupled to said I/Q demodulator.

18. The receiver according to claim 17, wherein said sampling rate control circuit stores a plurality of accumulated intersymbol carrier phase error differentials and computes a line of best fit therebetween.

19. The receiver according to claim 17, wherein said coupled output signal of said accumulator is enabled in said resampling circuit only during reception of a guard interval therein.

20. The receiver according to claim 17, wherein a common memory for storing output of said phase extraction circuit is coupled to said automatic frequency control circuit and to said automatic sampling rate control circuit.

21. The receiver according to claim 14, wherein said phase extraction circuit further comprises:

a pipelined circuit for iteratively computing the arctangent of an angle of rotation according to the series

$$\tan^{-1}(x) = x - \frac{x^3}{3} + \frac{x^5}{5} - \frac{x^7}{7} + \frac{x^9}{9} - \ldots, \qquad |x| < 1$$

wherein x is a ratio of said phase-uncorrected I and Q data.

22. The receiver according to claim 21, wherein said pipelined circuit comprises:

a constant coefficient multiplier; and

a multiplexer for selecting one of a plurality of constant coefficients of said series, an output of said multiplexer being connected to an input of said constant coefficient multiplier.

23. The receiver according to claim 21, wherein said pipelined circuit comprises:

a multiplier;

a first memory for storing the quantity x^2, said first memory being coupled to a first input of said multiplier;

a second memory for holding an output of said multiplier; and

a feedback connection between said second memory and a second input of said multiplier.

24. The receiver according to claim 21, wherein said pipelined circuit further comprises:

a third memory for storing a value of said series;

a control circuit, coupled to said third memory, wherein said pipeline circuit computes N terms of said series, and said pipeline circuit computes N+1 terms of said series, wherein N is an integer;

an averaging circuit coupled to said third memory for computing an average of said N terms and said N+1 terms of said series.

25. The receiver according to claim 1, wherein data transmitted in a pilot carrier of said multicarrier signal is BCH encoded according to a code generator polynomial h(x), further comprising:

a demodulator operative on said BCH encoded data;

an iterative pipelined BCH decoding circuit, comprising:

a circuit coupled to said demodulator for forming a Galois Field of said polynomial, and calculating a plurality of syndromes therewith;

a plurality of storage registers, each said storage register storing a respective one of said syndromes;

a plurality of feedback shift registers, each said feedback shift register accepting data from a respective one of said storage registers and having an output;

a plurality of Galois field multipliers, each said multiplier being connected in a feedback loop across a respective one of said feedback shift registers and multiplying the output of its associated feedback shift register by an alpha value of said Galois Field;

an output Galois field multiplier for multiplying said outputs of two of said feedback shift registers;

an error detection circuit connected to said feedback shift registers and said output Galois field multiplier, wherein an ouput signal of said error detection circuit indicates an error in a current bit of data; and

a feedback line enabled by said error detection circuit and connected to said storage registers, wherein outputs of said feedback shift registers are written into said storage registers.

26. The receiver according to claim 25, wherein said output Galois field multiplier comprises:

a first register initially storing a first multiplicand A;

a constant coefficient multiplier connected to said register for multiplication by a value α, an output of said constant coefficient multiplier being connected to said first register to define a first feedback loop, whereby in a kth cycle of clocked operation said first register contains a Galois field product $A\alpha^k$;

a second register for storing a second multiplicand B;

an AND gate connected to said second register and to said output of said constant coefficient multiplier;

an adder having a first input connected to an output of said AND gate;

an accumulator connected to a second input of said adder; wherein an output of said adder is connected to said accumulator to define a second feedback loop; whereby a Galois field product AB is output by said adder.

27. A method for estimation of a frequency response of a channel, comprising the steps of:

receiving from a channel a multicarrier signal having a plurality of data carriers and scattered pilot carriers, said scattered pilot carriers being spaced apart at a first interval N and being transmitted at a power that differs from a transmitted power of said data carriers;

converting said multicarrier signal to a digital representation thereof;

performing a Fourier transform on said digital representation of said multicarrier signal to generate a transformed digital signal;

reversing a bit order of said transformed digital signal to generate a bit-order reversed signal;

cyclically accumulating magnitudes of carriers in said bit-order reversed signal in N accumulators;

correlating said accumulated magnitudes with said power of said scattered pilot carriers;

responsive to said step of correlating, generating a synchronizing signal that identifies a carrier of said multicarrier signal.

28. The method according to claim 27, wherein said step of accumulating magnitudes comprises the steps of:

adding absolute values of a real component of said bit-order reversed signal to respective absolute values of imaginary components thereof to generate sums;

respectively storing said sums in said accumulators.

29. The method according to claim 27, wherein said step of correlating said accumulated magnitudes further comprises the step of:

identifying a first accumulator having a highest value stored therein representing a first carrier position.

30. The method according to claim 29, wherein said step of correlating said accumulated magnitudes further comprises the steps of:

identifying a second accumulator having a second highest value stored therein representing a second carrier position; and

determining an interval between said first carrier position and said second carrier position.

31. The method according to claim 27, further comprising the steps of:

comparing a position of a carrier of a first symbol in said bit-order reversed signal with a position of a carrier of a second symbol therein.

32. The method according to claim 27, further comprising the steps of:

interpolating between pilot carriers to determine correction factors for respective intermediate data carriers disposed therebetween; and

respectively adjusting magnitudes of said intermediate data carriers according to said correction factors.

33. The method according to claim 27, further comprising the steps of:

determining a mean phase difference between corresponding pilot carriers of successive symbols being transmitted in said transformed digital signal; and

generating a first control signal responsive to said mean phase difference; and

responsive to said first control signal adjusting a frequency of reception of said multicarrier signal.

34. The method according to claim 33, further comprising the steps of:

determining a first phase difference between a first data carrier of a first symbol in said transmitted data carrier and said first data carrier of a second symbol therein;

determining a second phase difference between a second data carrier of said first symbol and said second data carrier of said second symbol; and

determining a difference between said first phase difference and said second phase difference to define a phase slope between said first data carrier and said second data carrier;

generating a second control signal responsive to said phase slope; and

responsive to said second control signal adjusting a sampling frequency of said multicarrier signal.

35. The method according to claim 34, wherein said step of determining a difference between said first phase difference and said second phase difference comprises computing a line of best fit.

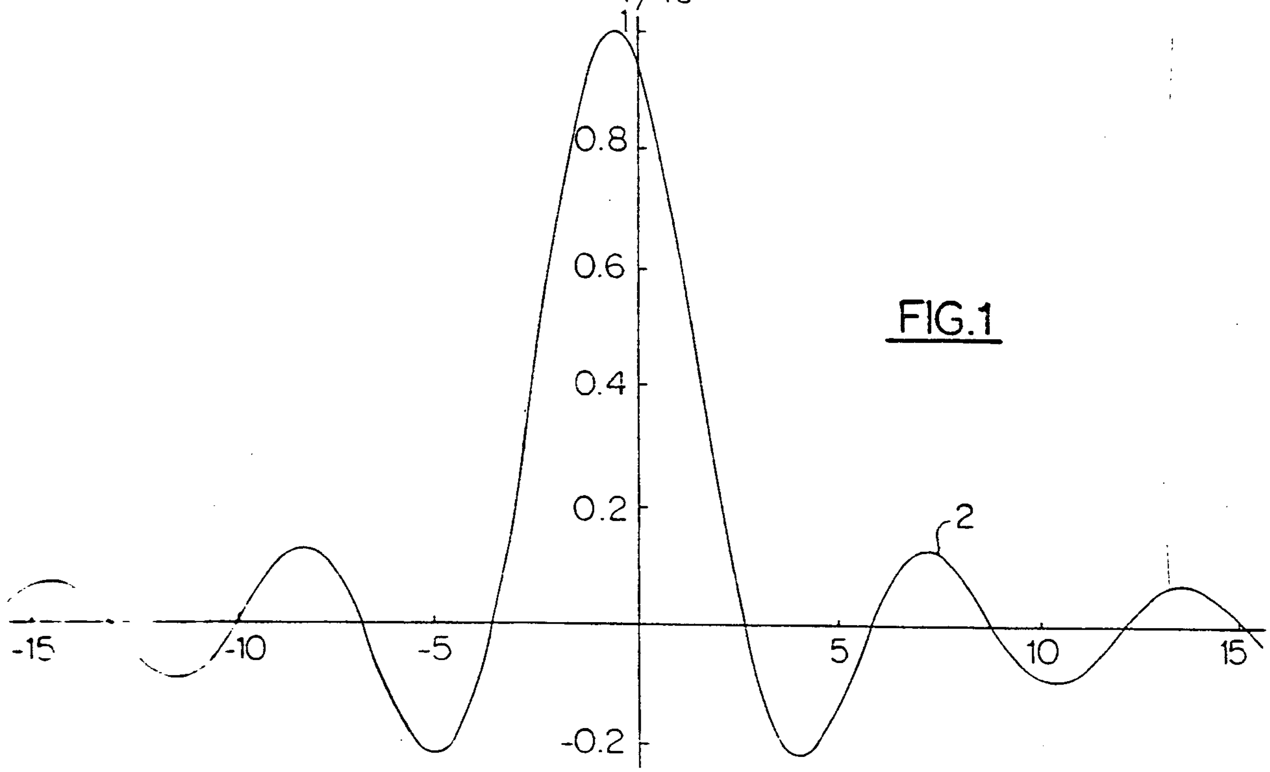


FIG.1

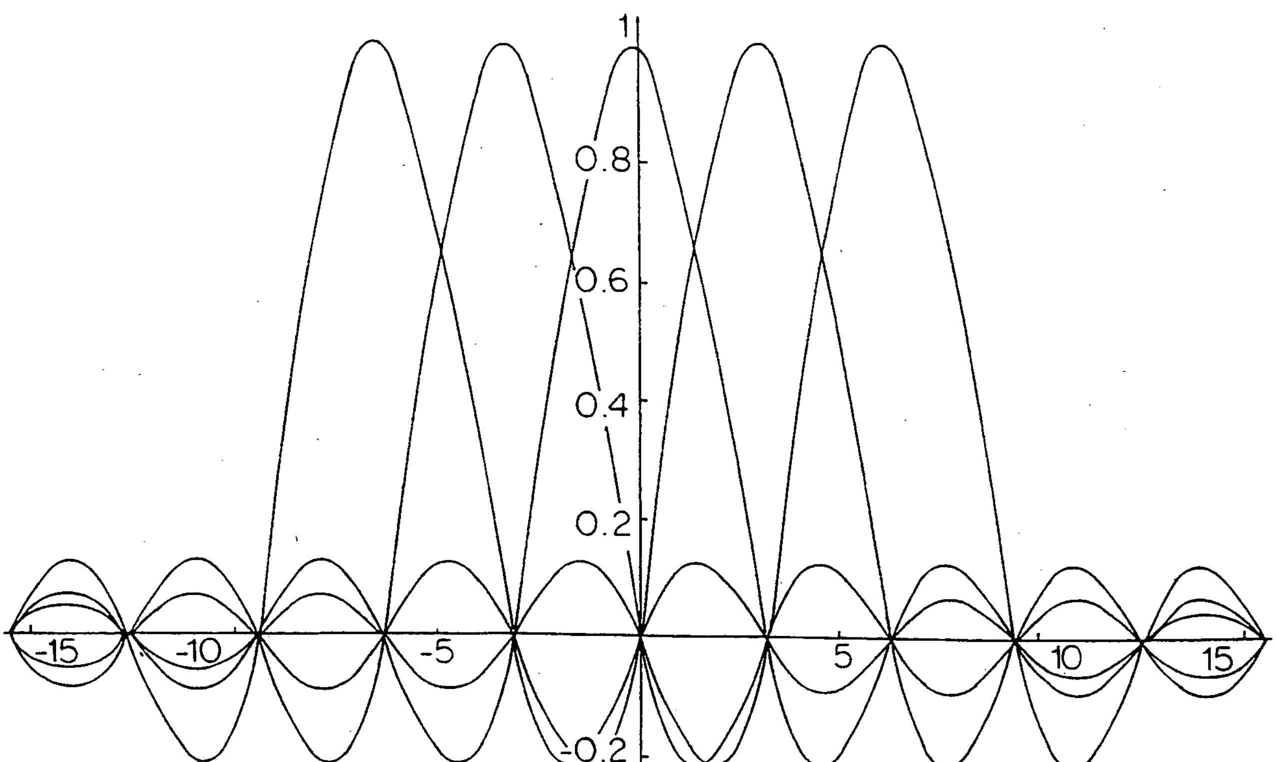


FIG.2

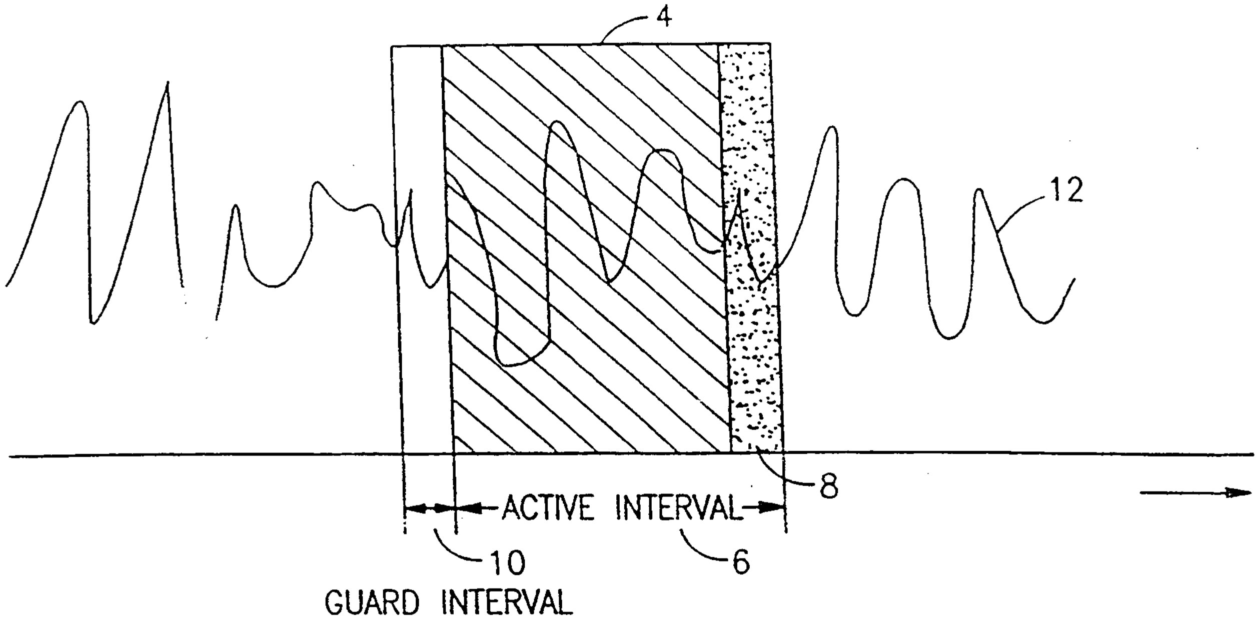

SYMBOL M-1
SYMBOL M
SYMBOL M+1
4
12
8
ACTIVE INTERVAL
10
6
GUARD INTERVAL

FIG.3

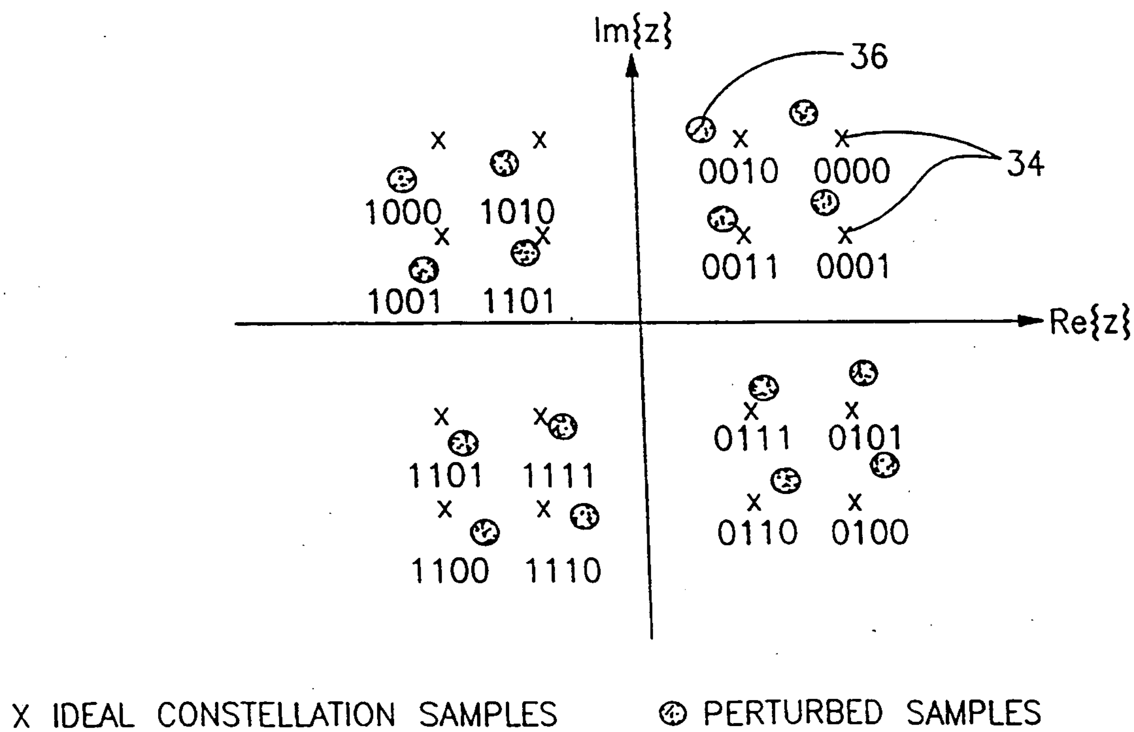

Im{z}
36
34
0010
0000
0011
0001
1000
1010
1001
1101
Re{z}
0111
0101
0110
0100
1101
1111
1100
1110
X IDEAL CONSTELLATION SAMPLES
PERTURBED SAMPLES

FIG.5

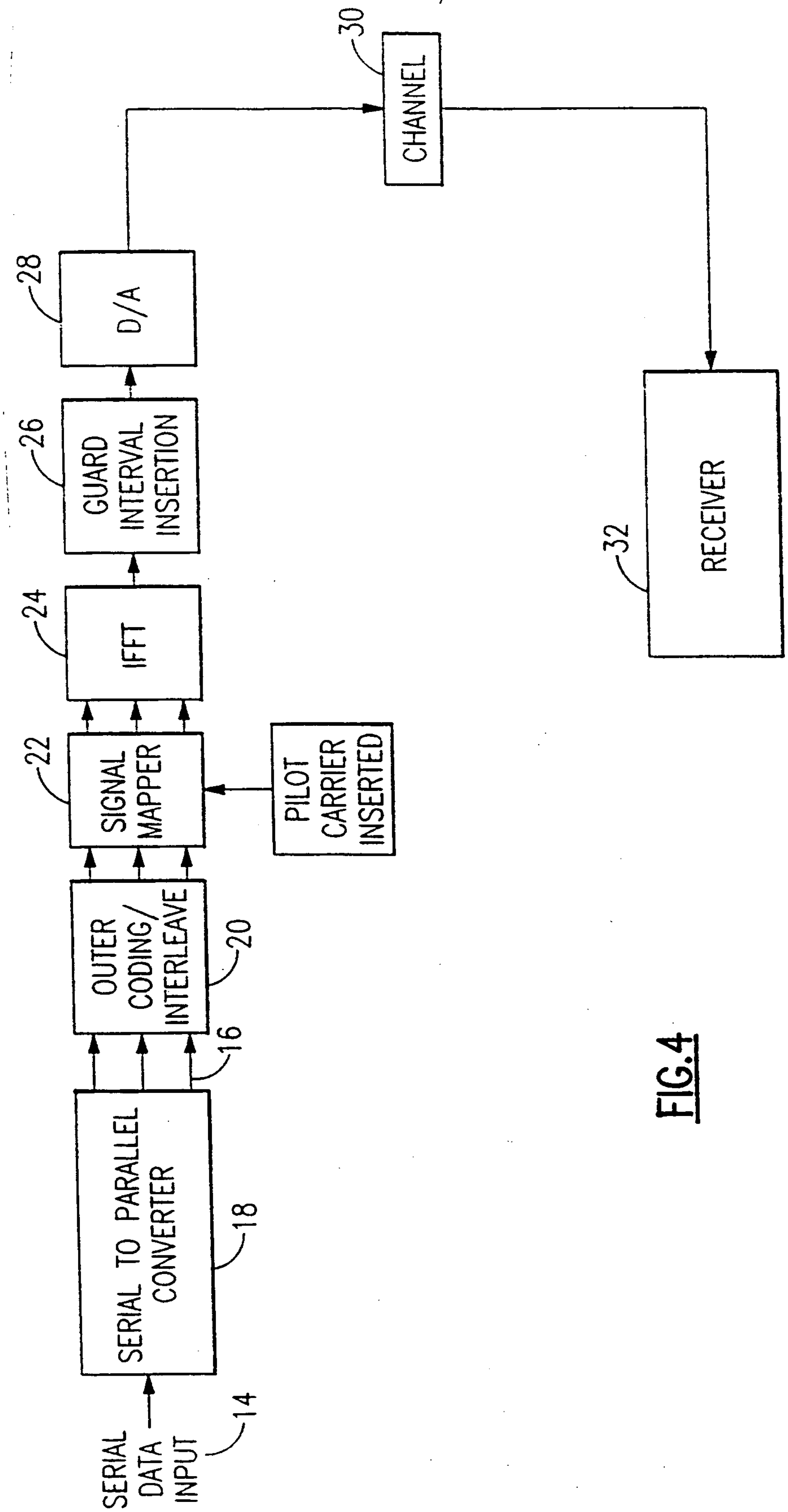

SERIAL DATA INPUT
14
SERIAL TO PARALLEL CONVERTER
18
16
OUTER CODING/ INTERLEAVE
20
SIGNAL MAPPER
22
PILOT CARRIER INSERTED
IFFT
24
GUARD INTERVAL INSERTION
26
D/A
28
CHANNEL
30
RECEIVER
32

FIG.4

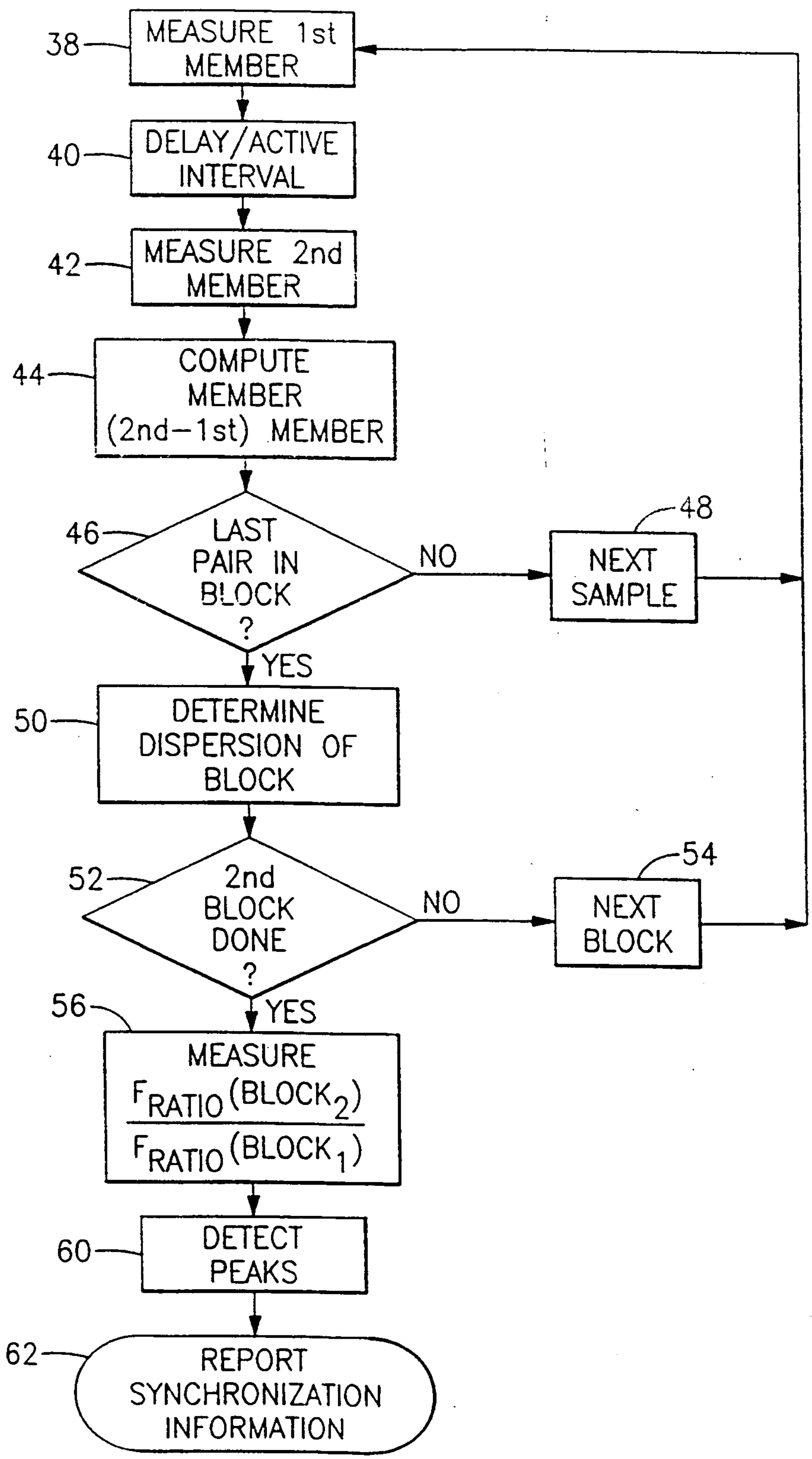

MEASURE 1st MEMBER
38
DELAY/ACTIVE INTERVAL
40
MEASURE 2nd MEMBER
42
COMPUTE MEMBER (2nd-1st) MEMBER
44
LAST PAIR IN BLOCK ?
46
NO
NEXT SAMPLE
48
YES
DETERMINE DISPERSION OF BLOCK
50
2nd BLOCK DONE ?
52
NO
NEXT BLOCK
54
YES
56
MEASURE $\frac{F_{RATIO}(BLOCK_2)}{F_{RATIO}(BLOCK_1)}$
DETECT PEAKS
60
REPORT SYNCHRONIZATION INFORMATION
62

FIG.6

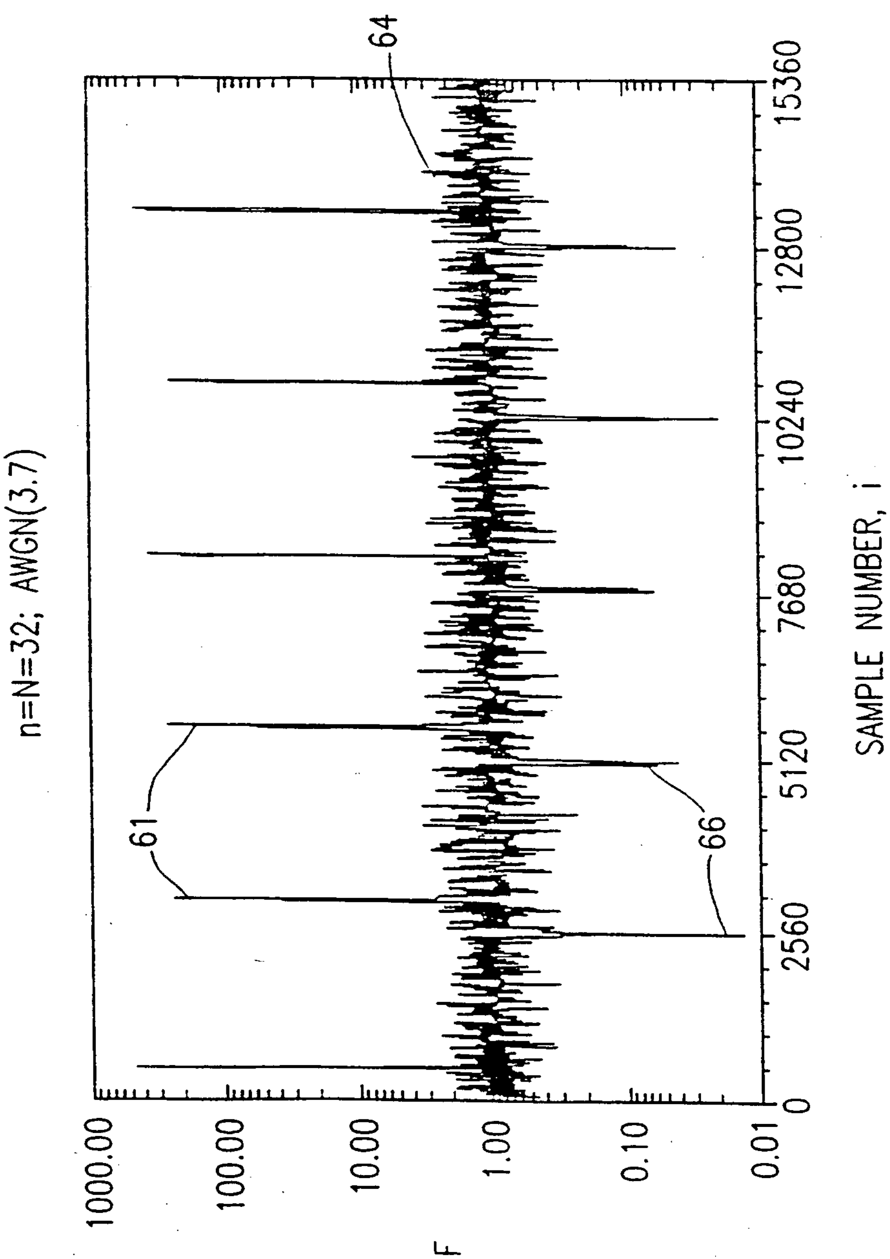

n=N=32; AWGN(3.7)
1000.00
100.00
10.00
1.00
0.10
0.01
F
0
2560
5120
7680
10240
12800
15360
SAMPLE NUMBER, i
61
64
66

FIG.7

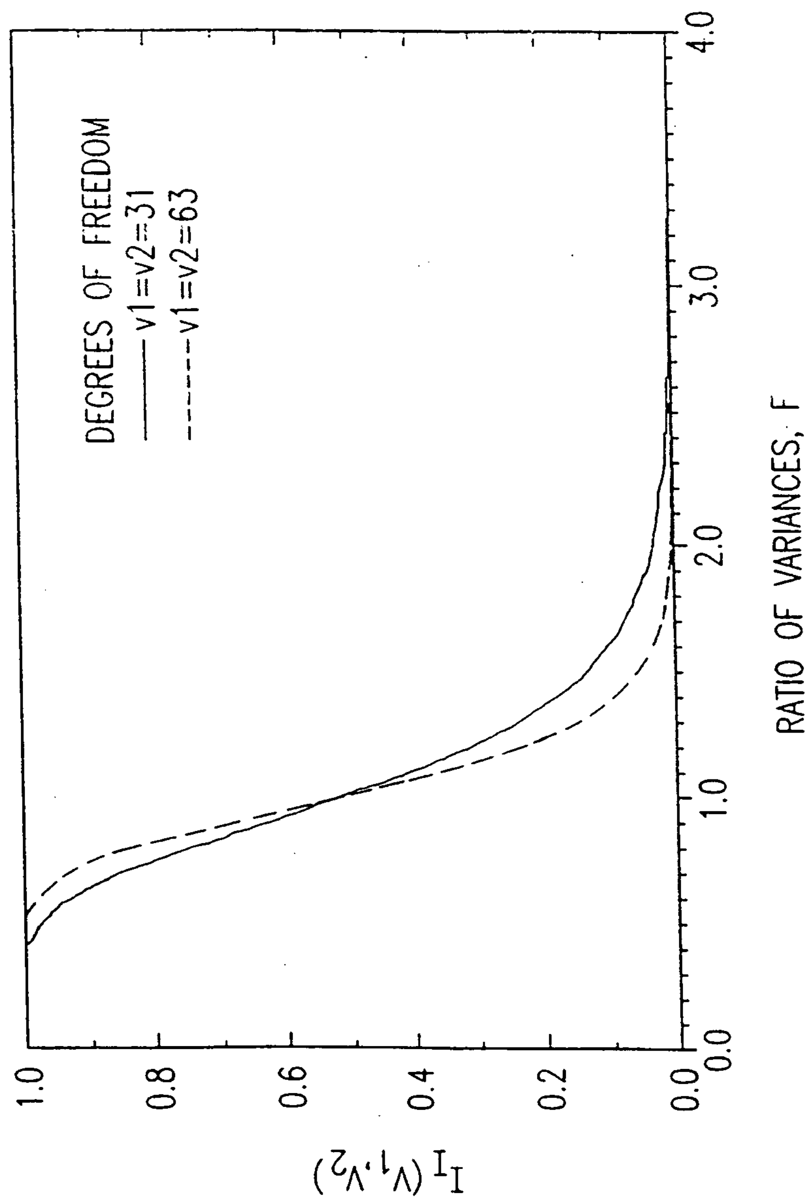

DEGREES OF FREEDOM
v1=v2=31
v1=v2=63
RATIO OF VARIANCES, F
$I_I (V_1,V_2)$
0.0
1.0
2.0
3.0
4.0
0.0
0.2
0.4
0.6
0.8
1.0

FIG.8

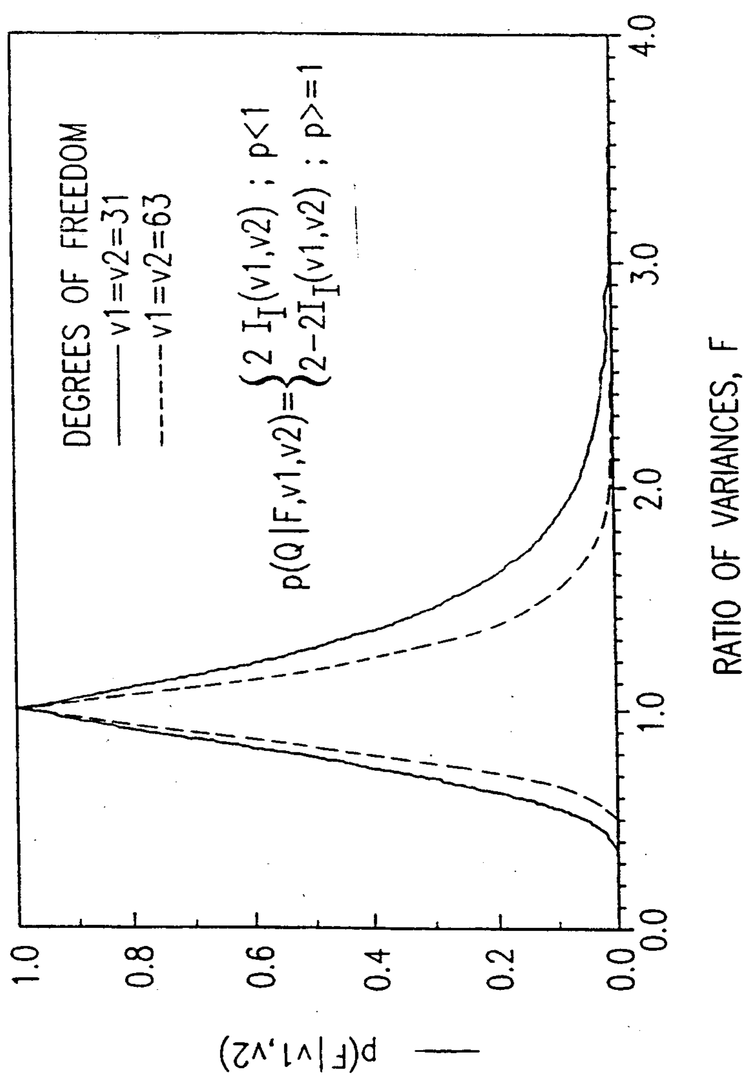

DEGREES OF FREEDOM
v1=v2=31
v1=v2=63
$p(Q|F,v1,v2)=\begin{cases} 2\ I_I(v1,v2)\ ;\ p<1 \\ 2-2I_I(v1,v2)\ ;\ p>=1 \end{cases}$
1.0
0.8
0.6
0.4
0.2
0.0
0.0
1.0
2.0
3.0
4.0
p(F|v1,v2)
RATIO OF VARIANCES, F

FIG.9

$$y/2 = \frac{\sum_{0}^{N-1} |S_{i-j}|}{\sum_{0}^{N-1} |S_{i-n-j}|}$$

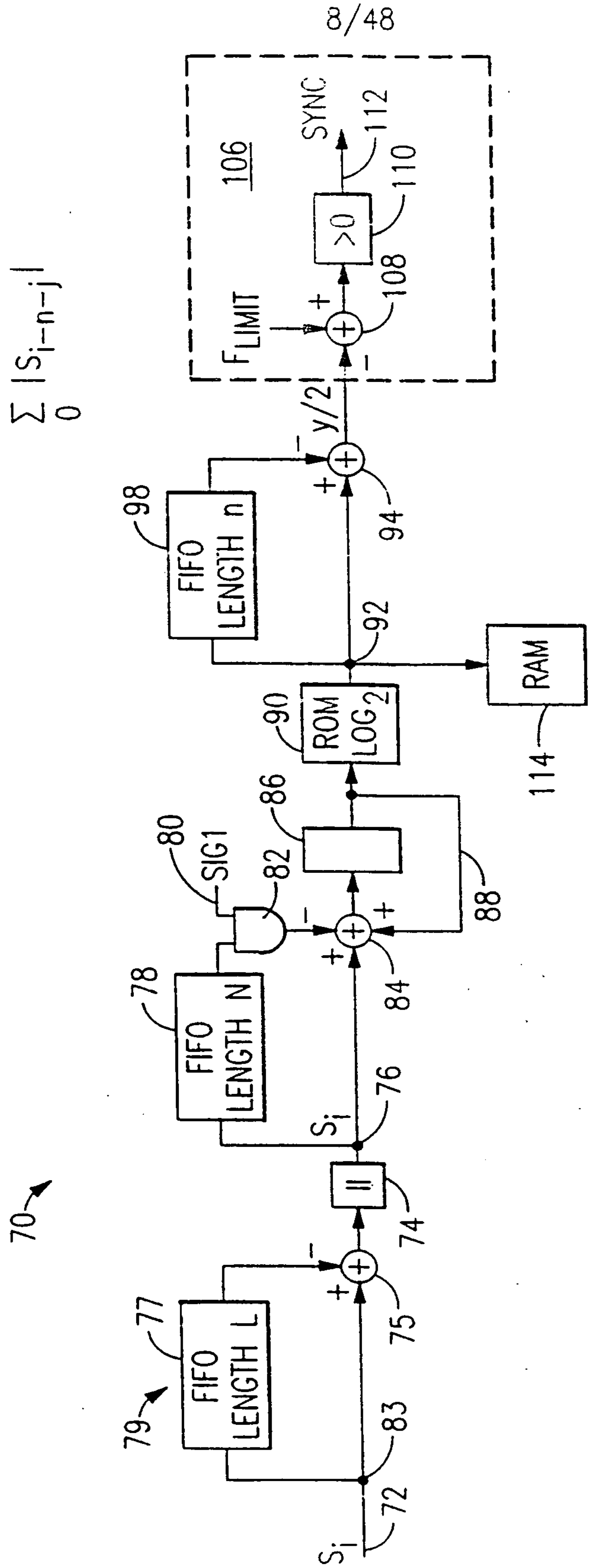


FIG.10

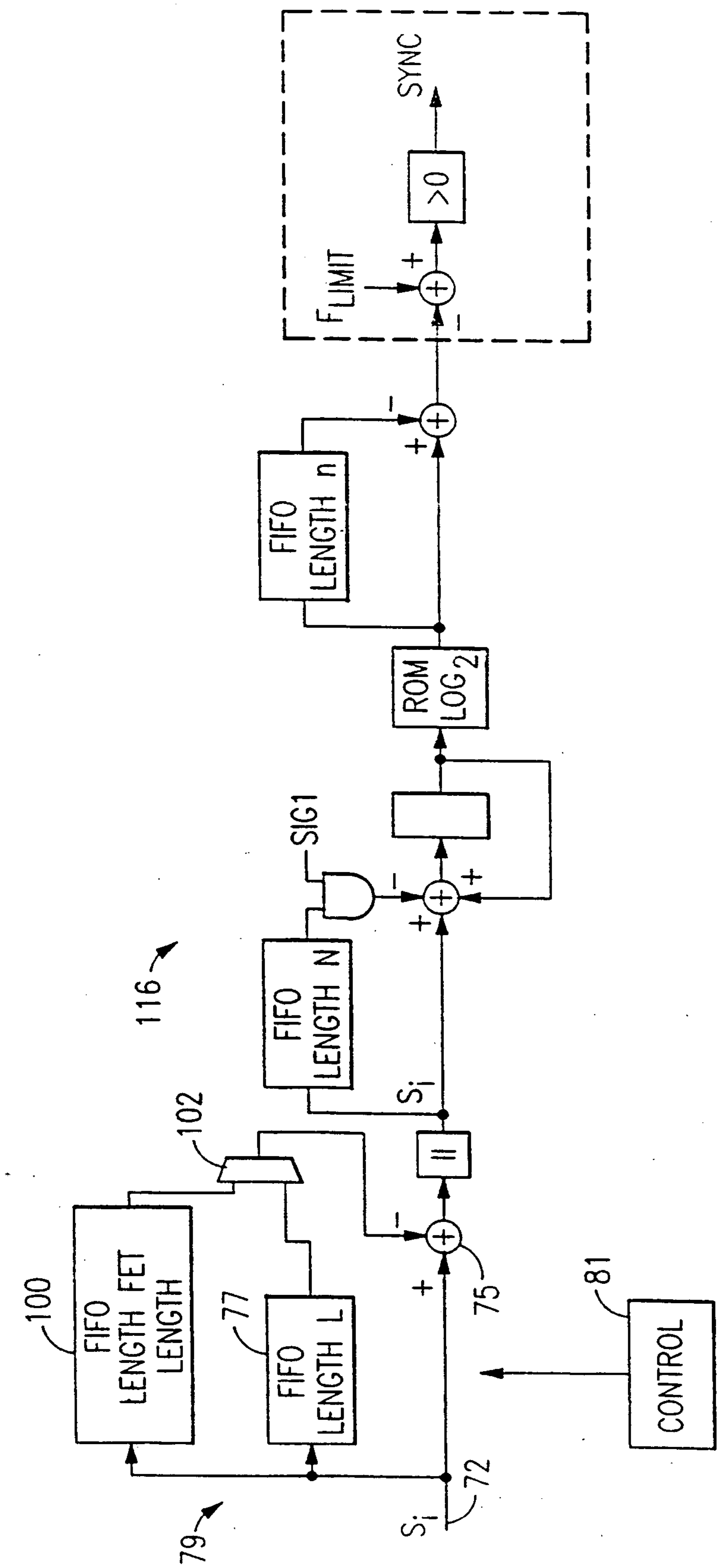

SYNC
>0
F_{LIMIT}
+
−
FIFO LENGTH n
ROM LOG$_2$
SIG1
116
FIFO LENGTH N
S_i
102
FIFO LENGTH FET LENGTH
100
77
FIFO LENGTH L
75
81
CONTROL
72
S_i
79

FIG.11

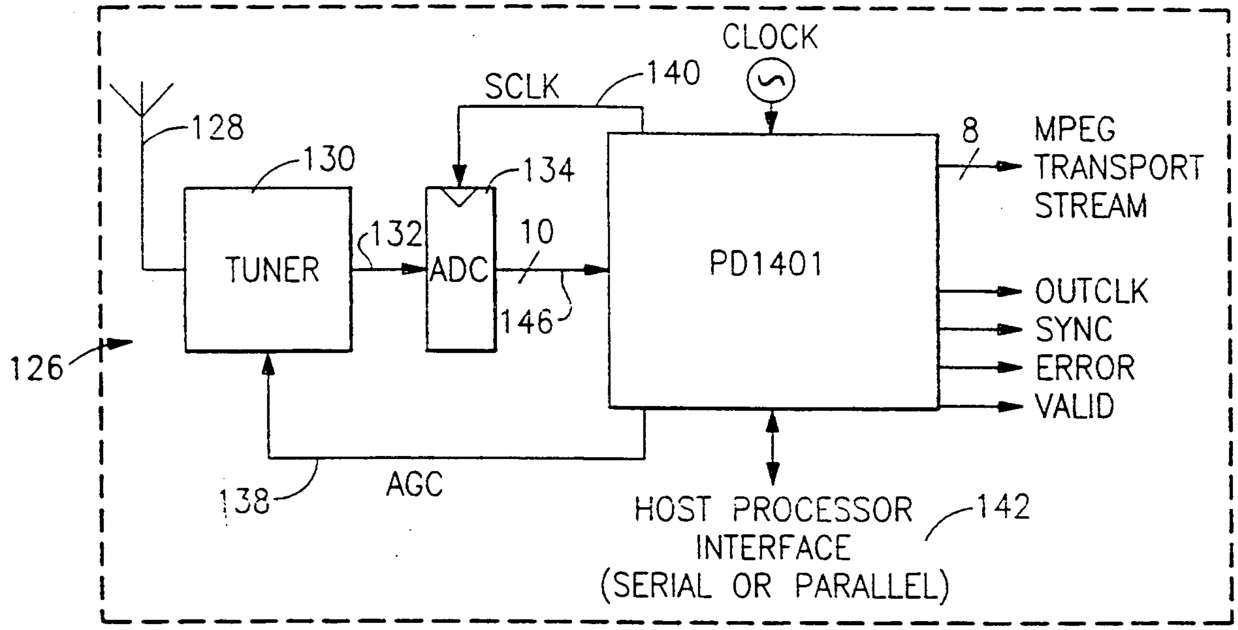

CLOCK
SCLK
140
128
130
134
8
MPEG TRANSPORT STREAM
TUNER
132
ADC
10
PD1401
146
OUTCLK
SYNC
ERROR
VALID
126
138
AGC
HOST PROCESSOR INTERFACE (SERIAL OR PARALLEL)
142

FIG.12

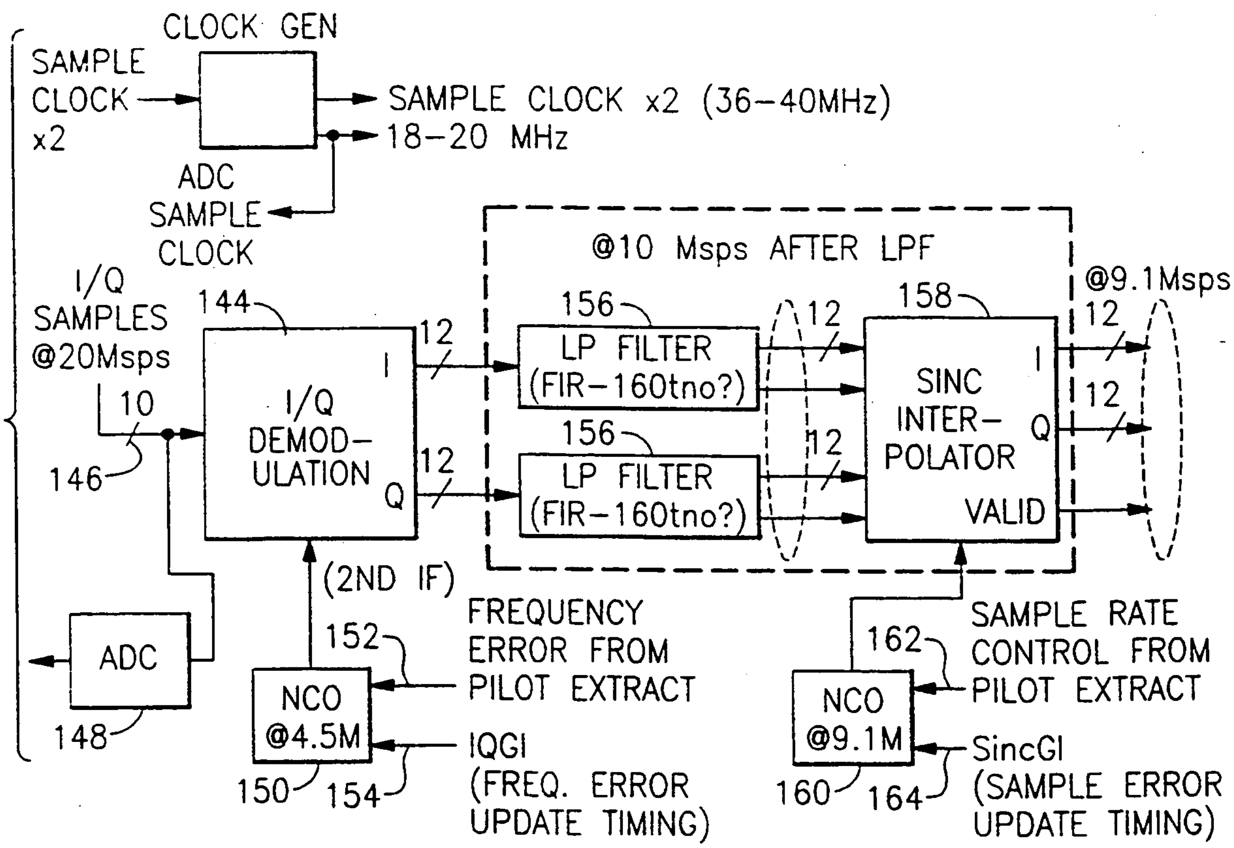

CLOCK GEN
SAMPLE CLOCK x2
SAMPLE CLOCK x2 (36-40MHz)
18-20 MHz
ADC SAMPLE CLOCK
@10 Msps AFTER LPF
I/Q SAMPLES @20Msps
144
12
156
LP FILTER (FIR-160tno?)
12
158
@9.1Msps
12
I
SINC INTER-POLATOR
12
10
I/Q DEMOD-ULATION
Q
146
12
156
LP FILTER (FIR-160tno?)
12
Q
VALID
(2ND IF)
FREQUENCY ERROR FROM PILOT EXTRACT
152
SAMPLE RATE CONTROL FROM PILOT EXTRACT
162
ADC
NCO @4.5M
NCO @9.1M
148
IQGI (FREQ. ERROR UPDATE TIMING)
SincGI (SAMPLE ERROR UPDATE TIMING)
150
154
160
164

FIG.13

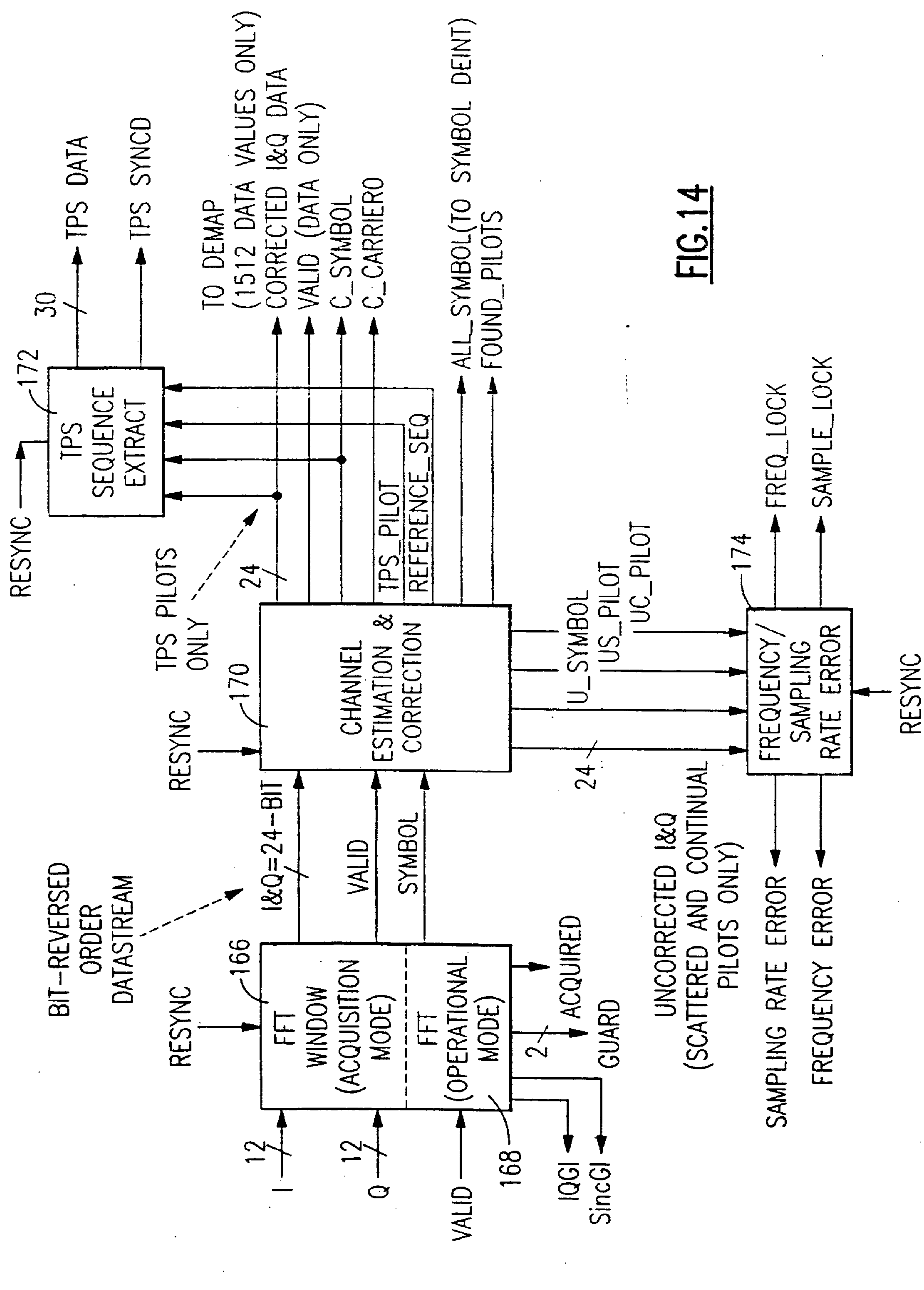

TPS DATA
TPS SYNCD
30
172
TPS SEQUENCE EXTRACT
RESYNC
TO DEMAP
(1512 DATA VALUES ONLY)
CORRECTED I&Q DATA
VALID (DATA ONLY)
C_SYMBOL
C_CARRIERO
ALL_SYMBOL(TO SYMBOL DEINT)
FOUND_PILOTS
TPS_PILOT
REFERENCE_SEQ
TPS PILOTS ONLY
24
170
RESYNC
CHANNEL ESTIMATION & CORRECTION
U_SYMBOL
US_PILOT
UC_PILOT
24
174
FREQ_LOCK
SAMPLE_LOCK
FREQUENCY/ SAMPLING RATE ERROR
RESYNC
UNCORRECTED I&Q
(SCATTERED AND CONTINUAL PILOTS ONLY)
SAMPLING RATE ERROR
FREQUENCY ERROR
BIT-REVERSED ORDER DATASTREAM
I&Q=24-BIT
VALID
SYMBOL
RESYNC
166
FFT WINDOW (ACQUISITION MODE)
FFT (OPERATIONAL MODE)
168
ACQUIRED
2
GUARD
12
I
12
Q
VALID
IQGI
SincGI

FIG.14

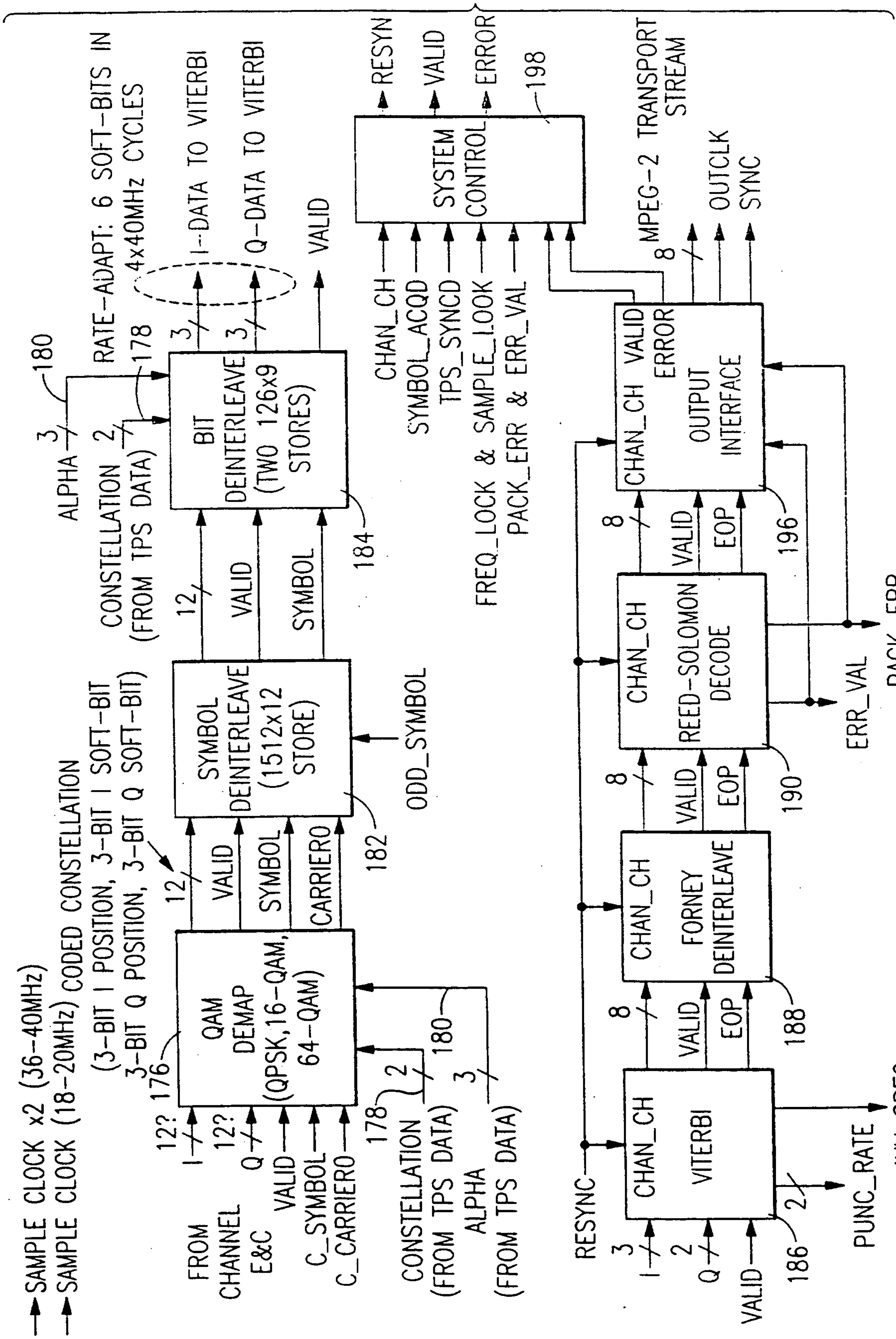

SAMPLE CLOCK x2 (36–40MHz)
SAMPLE CLOCK (18–20MHz)
FROM CHANNEL E&C
I
Q
12?
VALID
C_SYMBOL
C_CARRIER0
CONSTELLATION (FROM TPS DATA)
ALPHA (FROM TPS DATA)
178
180
2
3
QAM DEMAP (QPSK,16–QAM, 64–QAM)
176
CODED CONSTELLATION (3-BIT I POSITION, 3-BIT I SOFT-BIT 3-BIT Q POSITION, 3-BIT Q SOFT-BIT)
12
VALID
SYMBOL
CARRIER0
SYMBOL DEINTERLEAVE (1512x12 STORE)
182
ODD_SYMBOL
SYMBOL
BIT DEINTERLEAVE (TWO 126x9 STORES)
184
ALPHA
CONSTELLATION (FROM TPS DATA)
RATE–ADAPT: 6 SOFT–BITS IN 4x40MHz CYCLES
I–DATA TO VITERBI
Q–DATA TO VITERBI
SYSTEM CONTROL
198
RESYN
ERROR
CHAN_CH
SYMBOL_ACQD
TPS_SYNCD
FREQ_LOCK & SAMPLE_LOOK
PACK_ERR & ERR_VAL
MPEG–2 TRANSPORT STREAM
OUTCLK
SYNC
RESYNC
CHAN_CH VITERBI
186
PUNC_RATE
INV_SPEC
CHAN_CH FORNEY DEINTERLEAVE
188
EOP
CHAN_CH REED–SOLOMON DECODE
190
ERR_VAL
PACK_ERR
CHAN_CH OUTPUT INTERFACE
196
CHAN_CH VALID ERROR

FIG.15

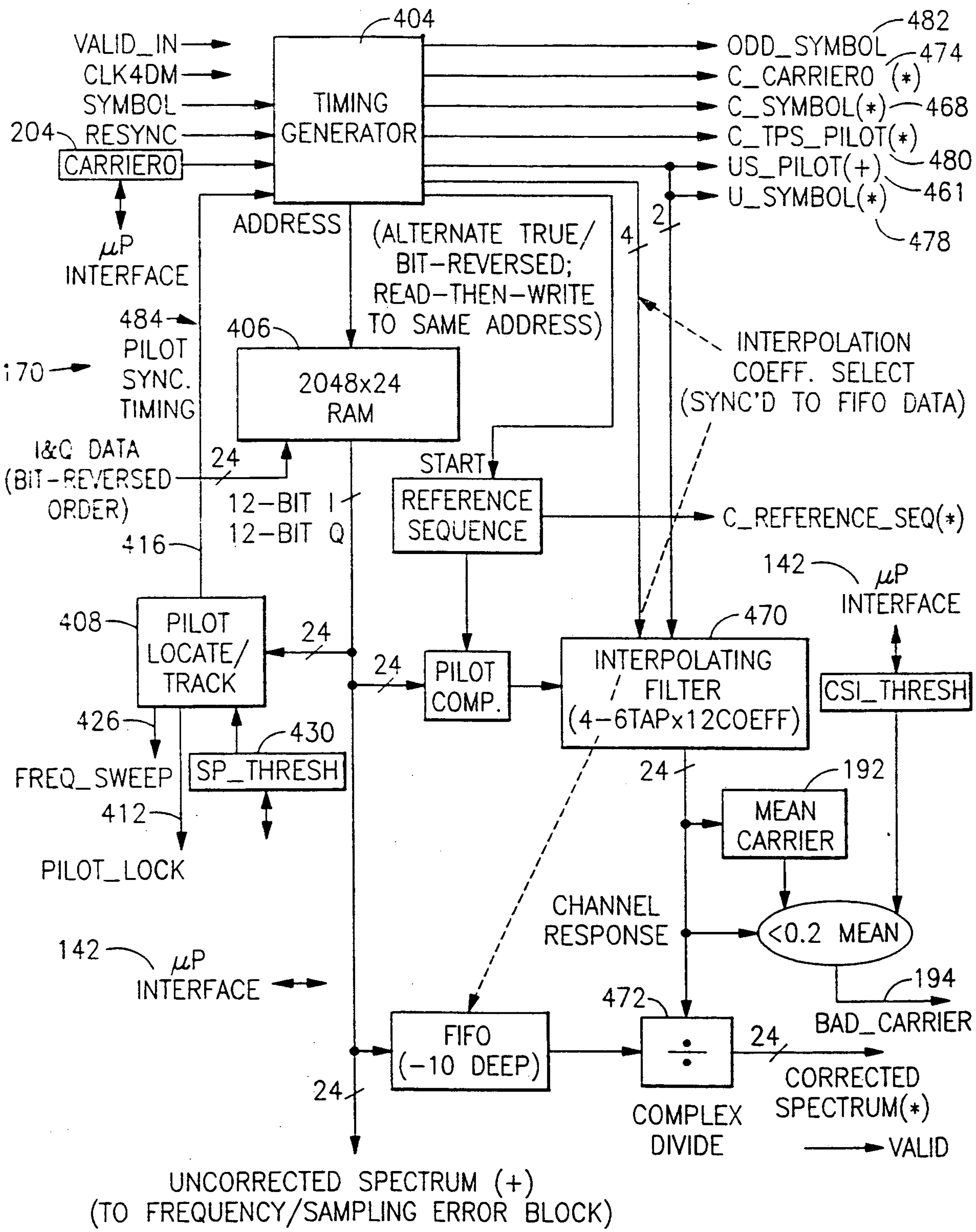

404
482
474
468
480
461
478
VALID_IN
CLK4DM
SYMBOL
RESYNC
204
CARRIER0
TIMING GENERATOR
ODD_SYMBOL
C_CARRIER0 (*)
C_SYMBOL(*)
C_TPS_PILOT(*)
US_PILOT(+)
U_SYMBOL(*)
μP INTERFACE
ADDRESS
(ALTERNATE TRUE/ BIT-REVERSED; READ-THEN-WRITE TO SAME ADDRESS)
4
2
484
PILOT SYNC. TIMING
170
406
2048x24 RAM
INTERPOLATION COEFF. SELECT (SYNC'D TO FIFO DATA)
I&Q DATA (BIT-REVERSED ORDER)
24
12-BIT I
12-BIT Q
START
REFERENCE SEQUENCE
C_REFERENCE_SEQ(*)
416
142
μP INTERFACE
408
PILOT LOCATE/ TRACK
24
24
PILOT COMP.
470
INTERPOLATING FILTER (4-6TAPx12COEFF)
CSI_THRESH
426
430
FREQ_SWEEP
SP_THRESH
24
192
412
MEAN CARRIER
PILOT_LOCK
CHANNEL RESPONSE
<0.2 MEAN
142
μP INTERFACE
194
472
BAD_CARRIER
FIFO (-10 DEEP)
24
CORRECTED SPECTRUM(*)
24
COMPLEX DIVIDE
VALID
UNCORRECTED SPECTRUM (+) (TO FREQUENCY/SAMPLING ERROR BLOCK)

FIG.16

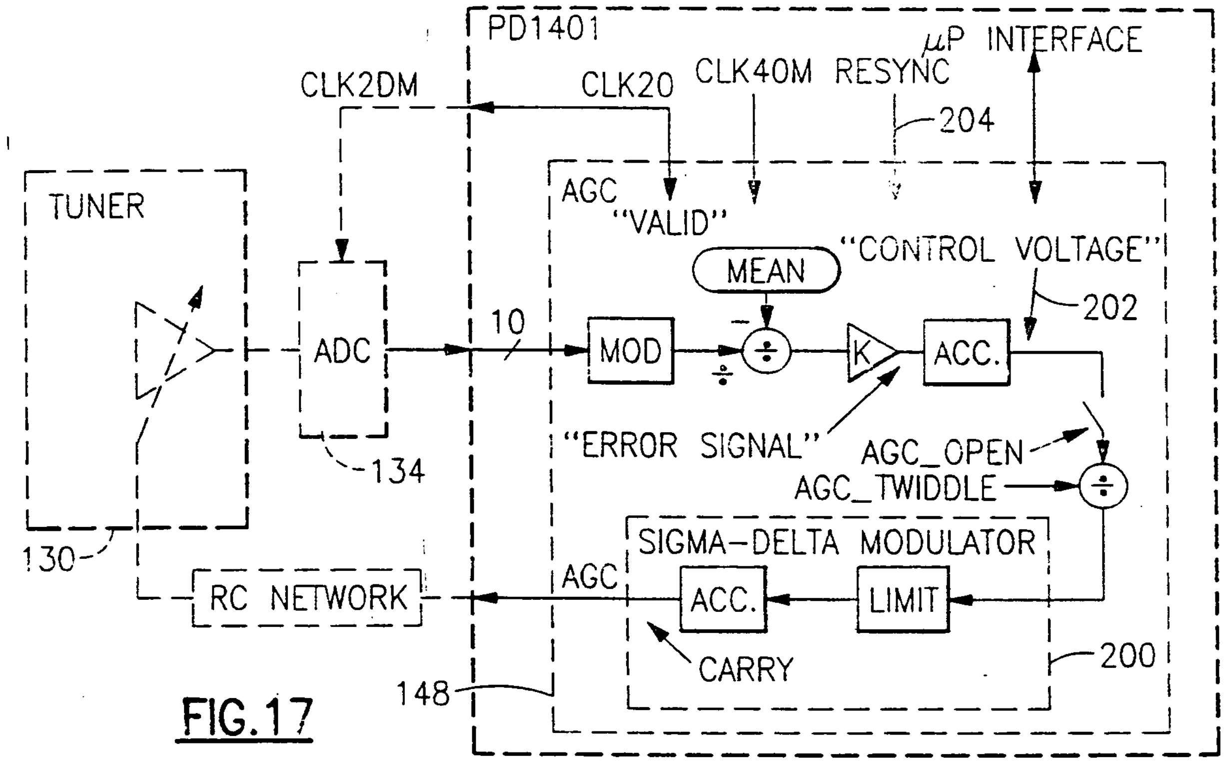

PD1401
CLK2DM
CLK20
CLK40M
RESYNC
μP INTERFACE
204
TUNER
ADC
134
130
AGC
"VALID"
MEAN
"CONTROL VOLTAGE"
202
10
MOD
K
ACC.
"ERROR SIGNAL"
AGC_OPEN
AGC_TWIDDLE
SIGMA-DELTA MODULATOR
RC NETWORK
AGC
ACC.
LIMIT
CARRY
200
148

FIG.17

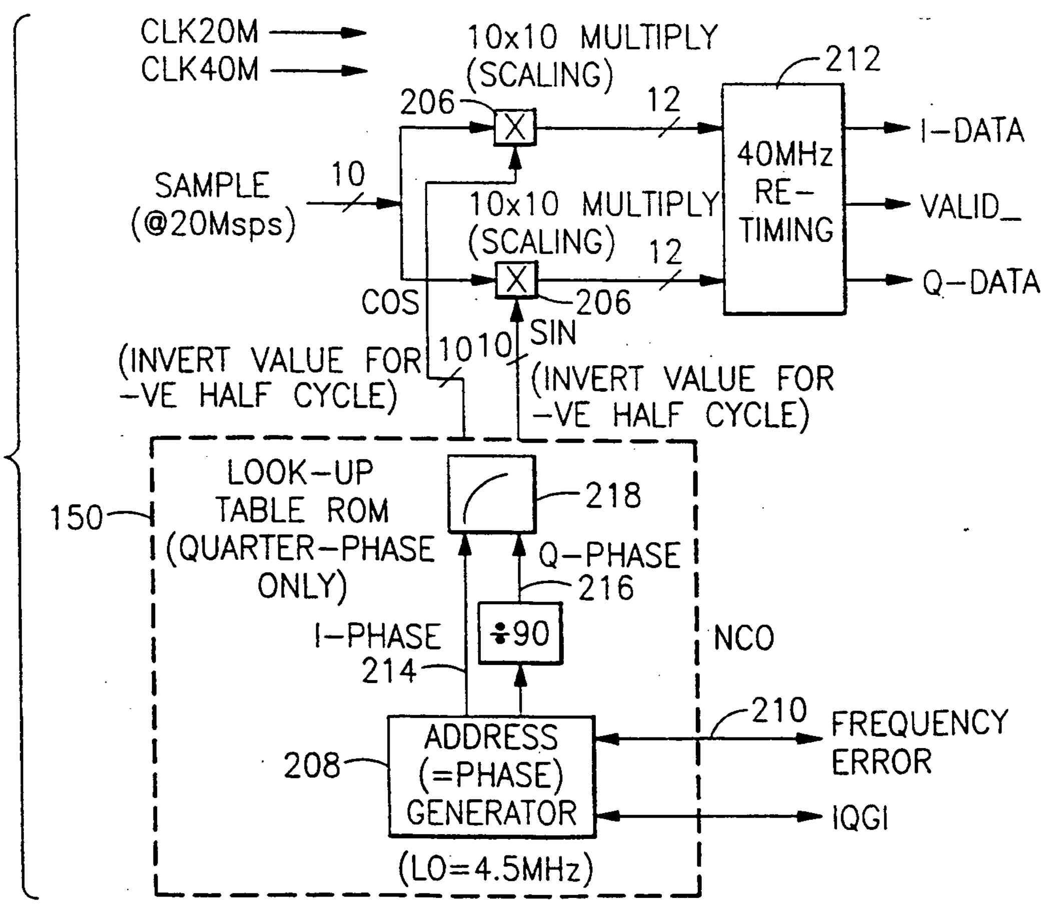

CLK20M
CLK40M
10x10 MULTIPLY (SCALING)
206
12
212
40MHz RE-TIMING
I-DATA
SAMPLE (@20Msps)
10
VALID_
Q-DATA
COS
SIN
(INVERT VALUE FOR -VE HALF CYCLE)
LOOK-UP TABLE ROM (QUARTER-PHASE ONLY)
218
Q-PHASE
216
150
I-PHASE
214
÷90
NCO
210
FREQUENCY ERROR
208
ADDRESS (=PHASE) GENERATOR
IQGI
(LO=4.5MHz)

FIG.18

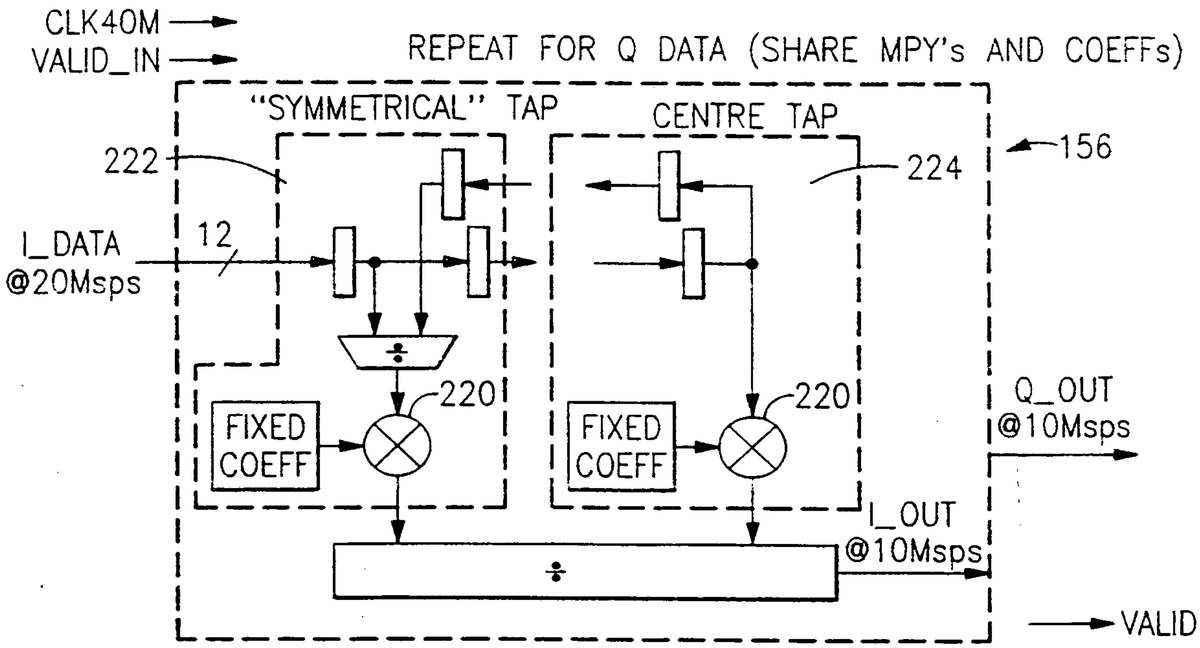

CLK40M
VALID_IN
REPEAT FOR Q DATA (SHARE MPY's AND COEFFs)
"SYMMETRICAL" TAP
CENTRE TAP
222
224
156
I_DATA
@20Msps
12
÷
220
220
FIXED
COEFF
FIXED
COEFF
Q_OUT
@10Msps
I_OUT
@10Msps
÷
VALID

FIG.19

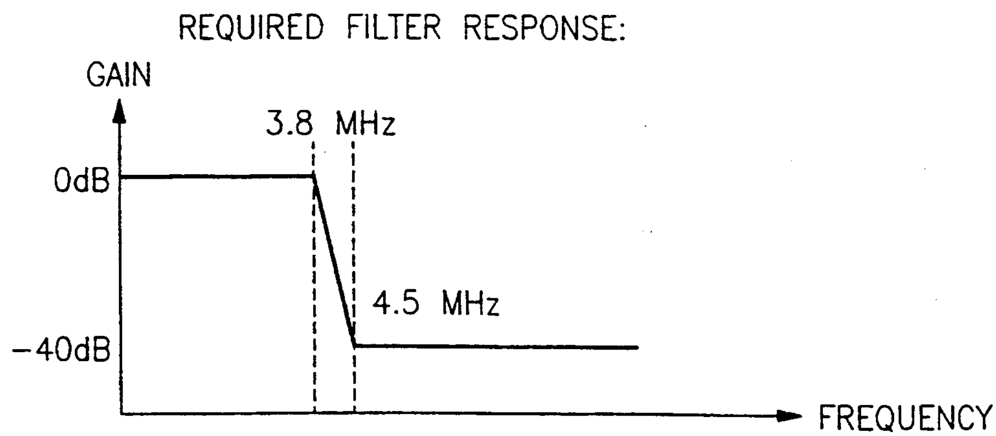

REQUIRED FILTER RESPONSE:
GAIN
3.8 MHz
0dB
4.5 MHz
−40dB
FREQUENCY

FIG.20

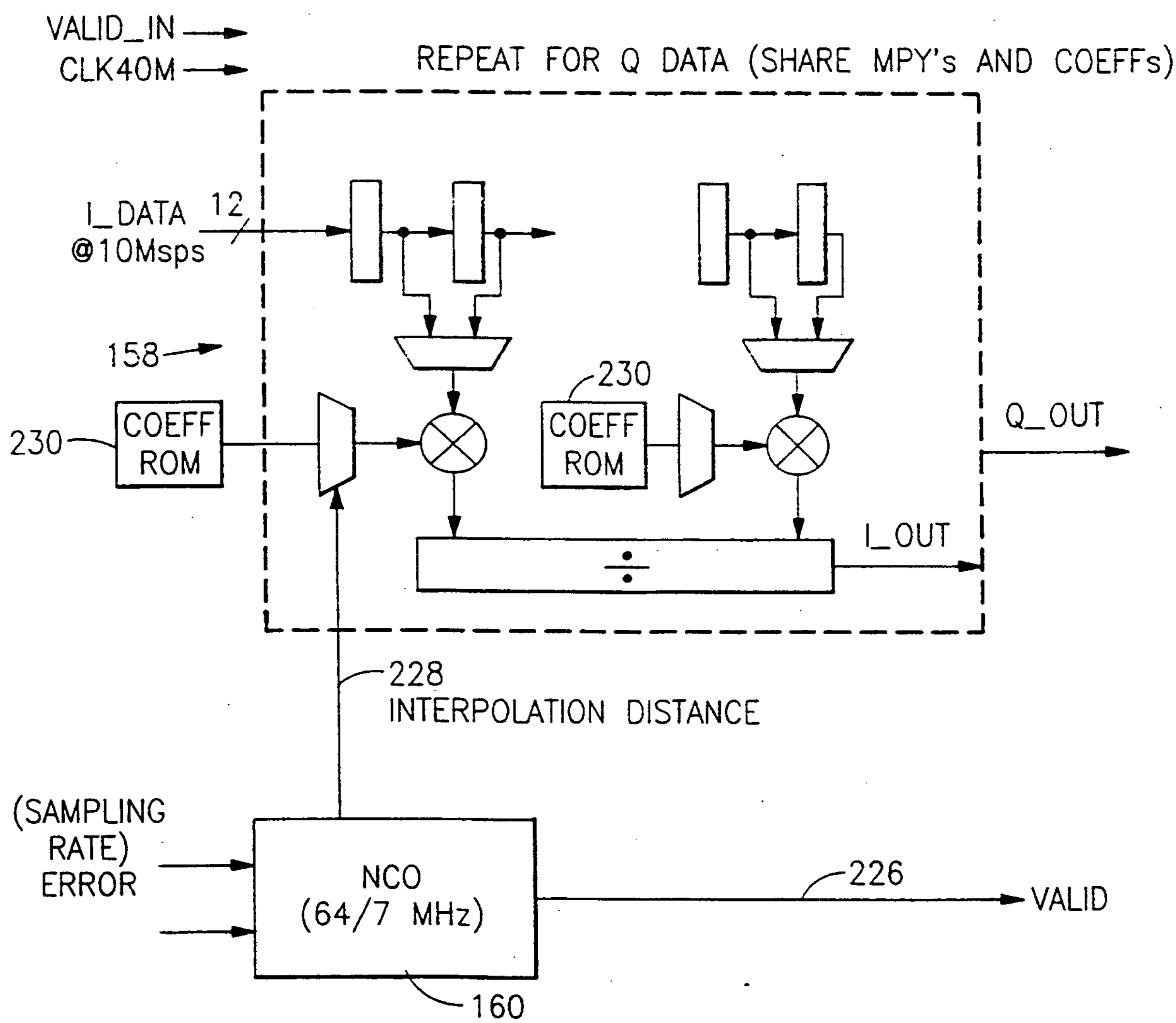
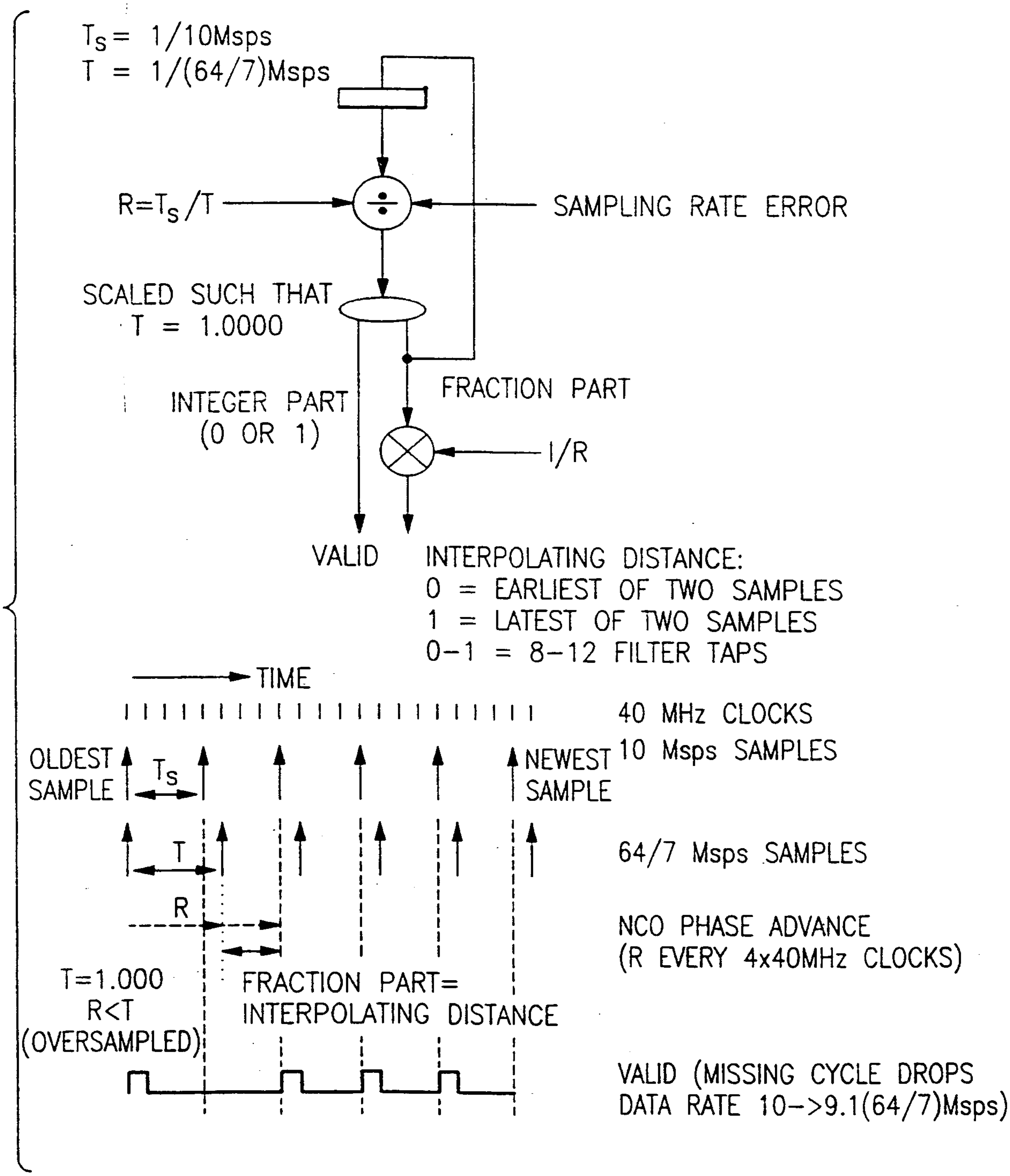

VALID_IN
CLK40M
REPEAT FOR Q DATA (SHARE MPY's AND COEFFs)
I_DATA
@10Msps
12
158
230
COEFF ROM
230
COEFF ROM
Q_OUT
I_OUT
÷
228
INTERPOLATION DISTANCE
(SAMPLING RATE) ERROR
NCO (64/7 MHz)
226
VALID
160

FIG.21



T_S = 1/10Msps
T = 1/(64/7)Msps
$R=T_S/T$
SAMPLING RATE ERROR
SCALED SUCH THAT
T = 1.0000
INTEGER PART
(0 OR 1)
FRACTION PART
I/R
VALID
INTERPOLATING DISTANCE:
0 = EARLIEST OF TWO SAMPLES
1 = LATEST OF TWO SAMPLES
0-1 = 8-12 FILTER TAPS
TIME
40 MHz CLOCKS
OLDEST SAMPLE
T_S
NEWEST SAMPLE
10 Msps SAMPLES
T
64/7 Msps SAMPLES
R
NCO PHASE ADVANCE
(R EVERY 4x40MHz CLOCKS)
T=1.000
R<T
(OVERSAMPLED)
FRACTION PART=
INTERPOLATING DISTANCE
VALID (MISSING CYCLE DROPS
DATA RATE 10->9.1(64/7)Msps)

FIG.22

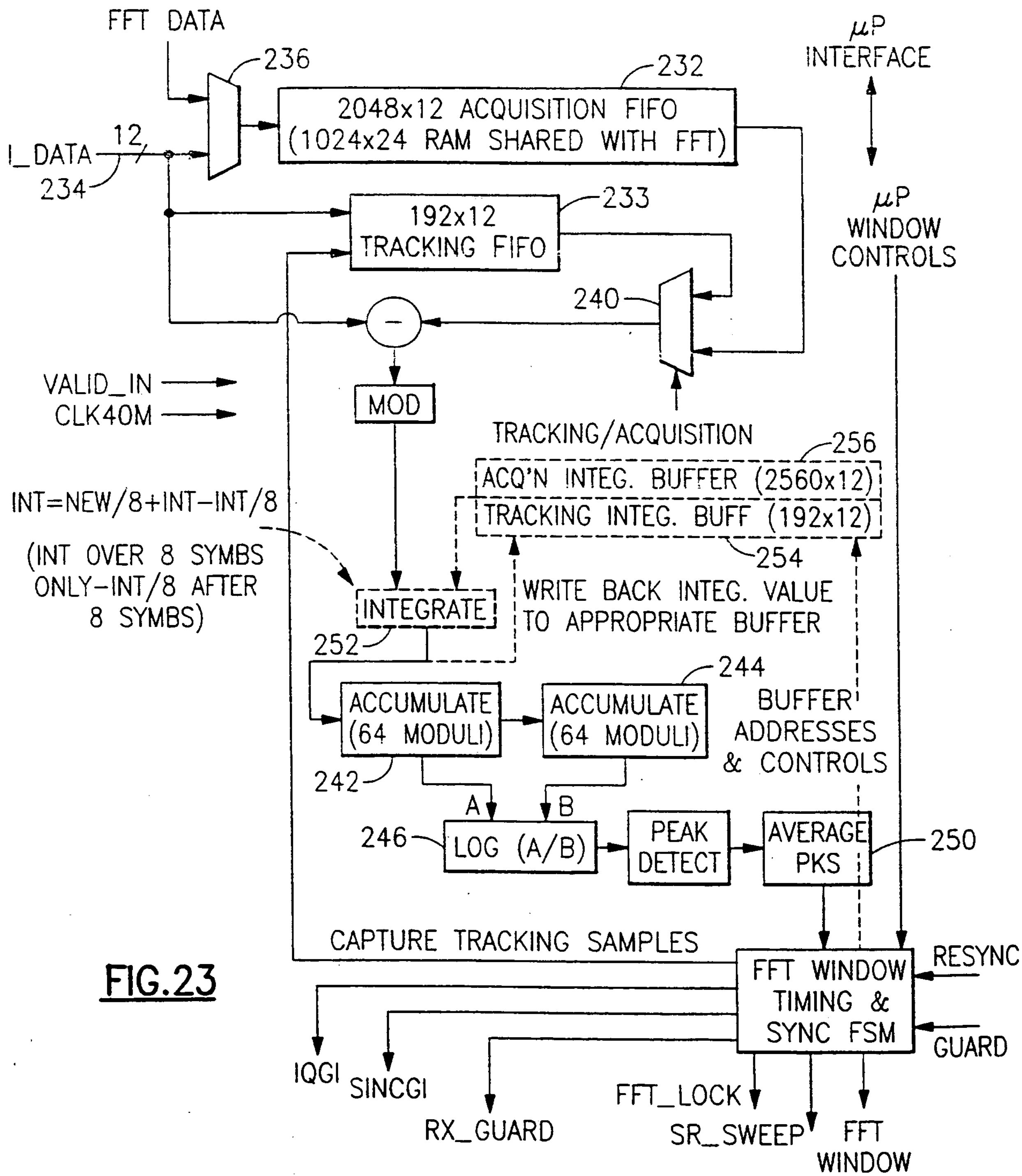

FFT DATA
236
232
2048x12 ACQUISITION FIFO
(1024x24 RAM SHARED WITH FFT)
μP
INTERFACE
I_DATA
12
234
192x12
TRACKING FIFO
233
μP
WINDOW
CONTROLS
240
–
VALID_IN
CLK40M
MOD
TRACKING/ACQUISITION
256
ACQ'N INTEG. BUFFER (2560x12)
TRACKING INTEG. BUFF (192x12)
254
INT=NEW/8+INT–INT/8
(INT OVER 8 SYMBS
ONLY–INT/8 AFTER
8 SYMBS)
INTEGRATE
WRITE BACK INTEG. VALUE
TO APPROPRIATE BUFFER
252
244
ACCUMULATE
(64 MODULI)
ACCUMULATE
(64 MODULI)
BUFFER
ADDRESSES
& CONTROLS
242
A
B
246
LOG (A/B)
PEAK
DETECT
AVERAGE
PKS
250
CAPTURE TRACKING SAMPLES
FFT WINDOW
TIMING &
SYNC FSM
RESYNC
GUARD
IQGI
SINCGI
RX_GUARD
FFT_LOCK
SR_SWEEP
FFT
WINDOW

FIG.23

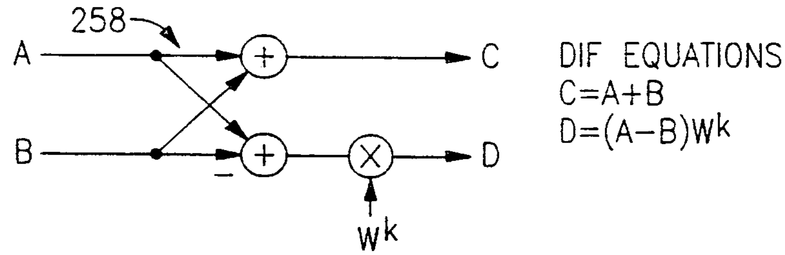


FIG.24

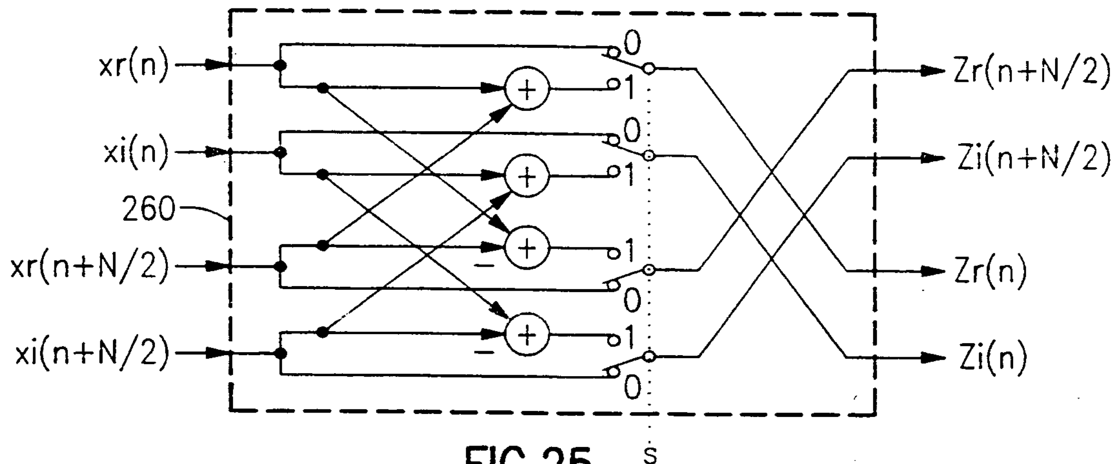


FIG.25
Prior Art

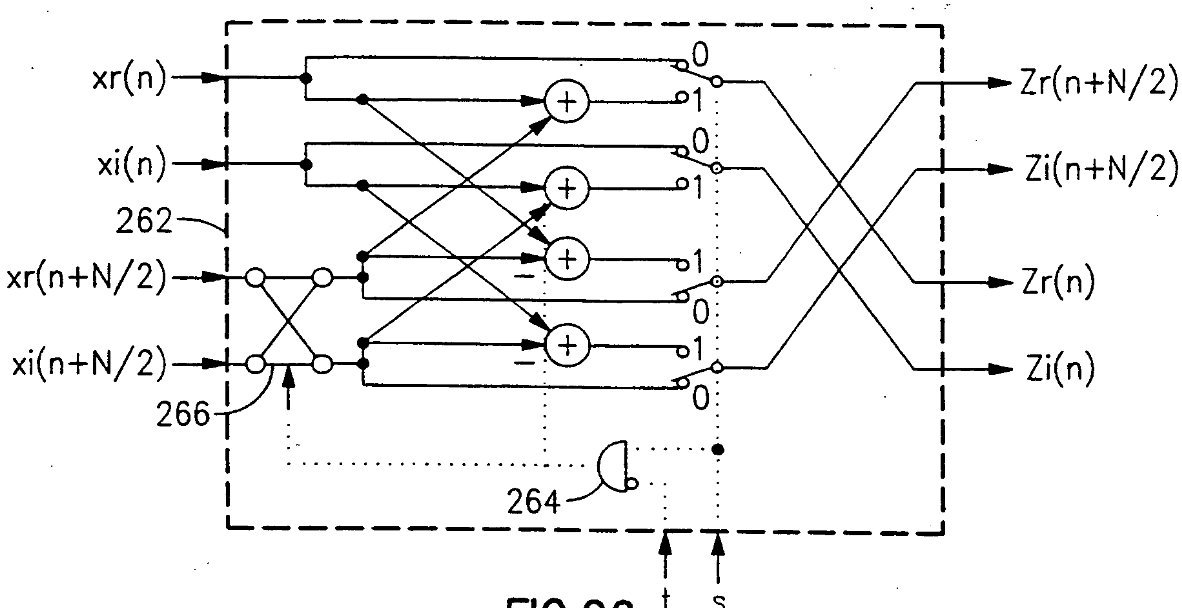


FIG.26
Prior Art

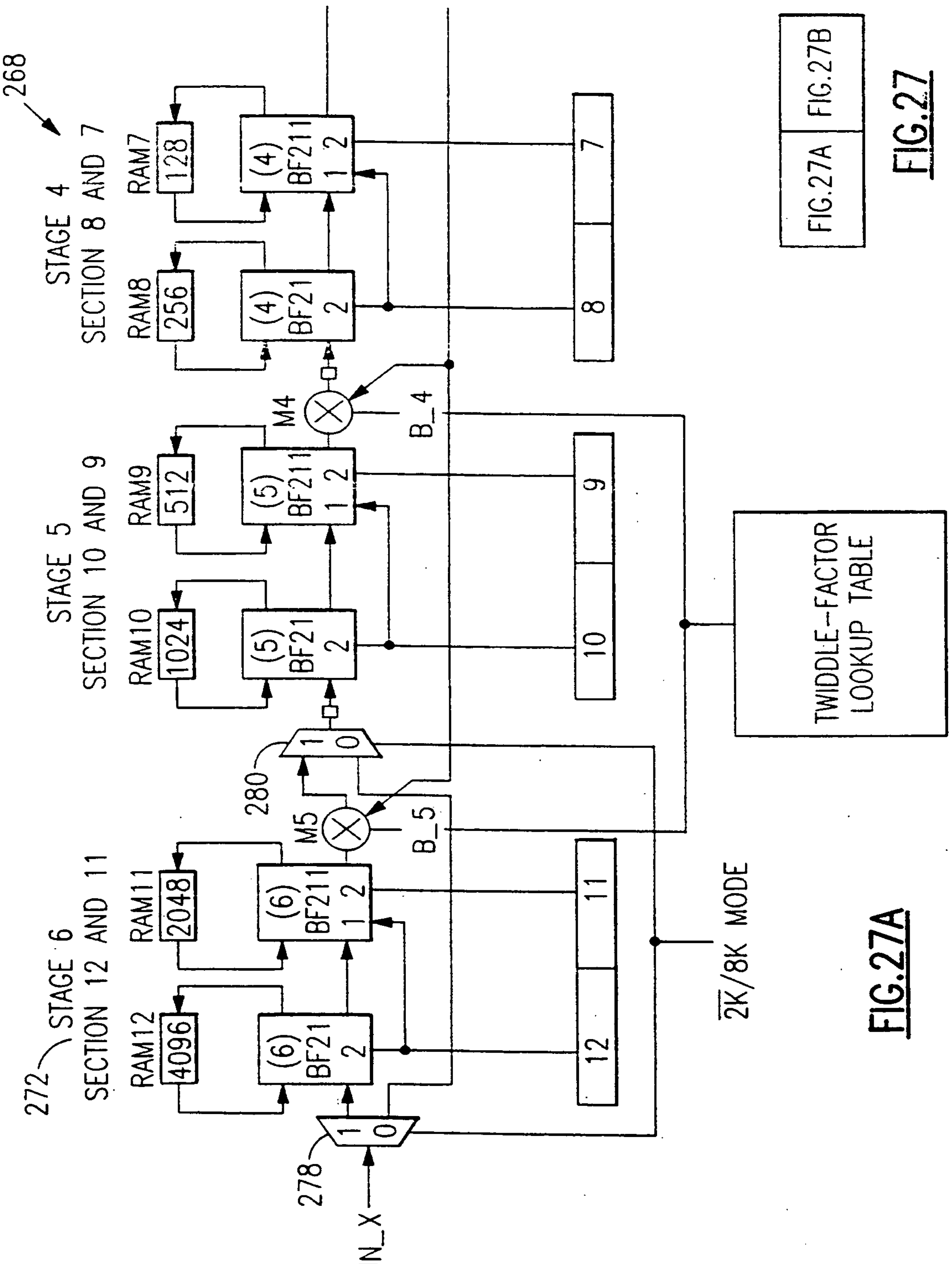


FIG.27A

FIG.27

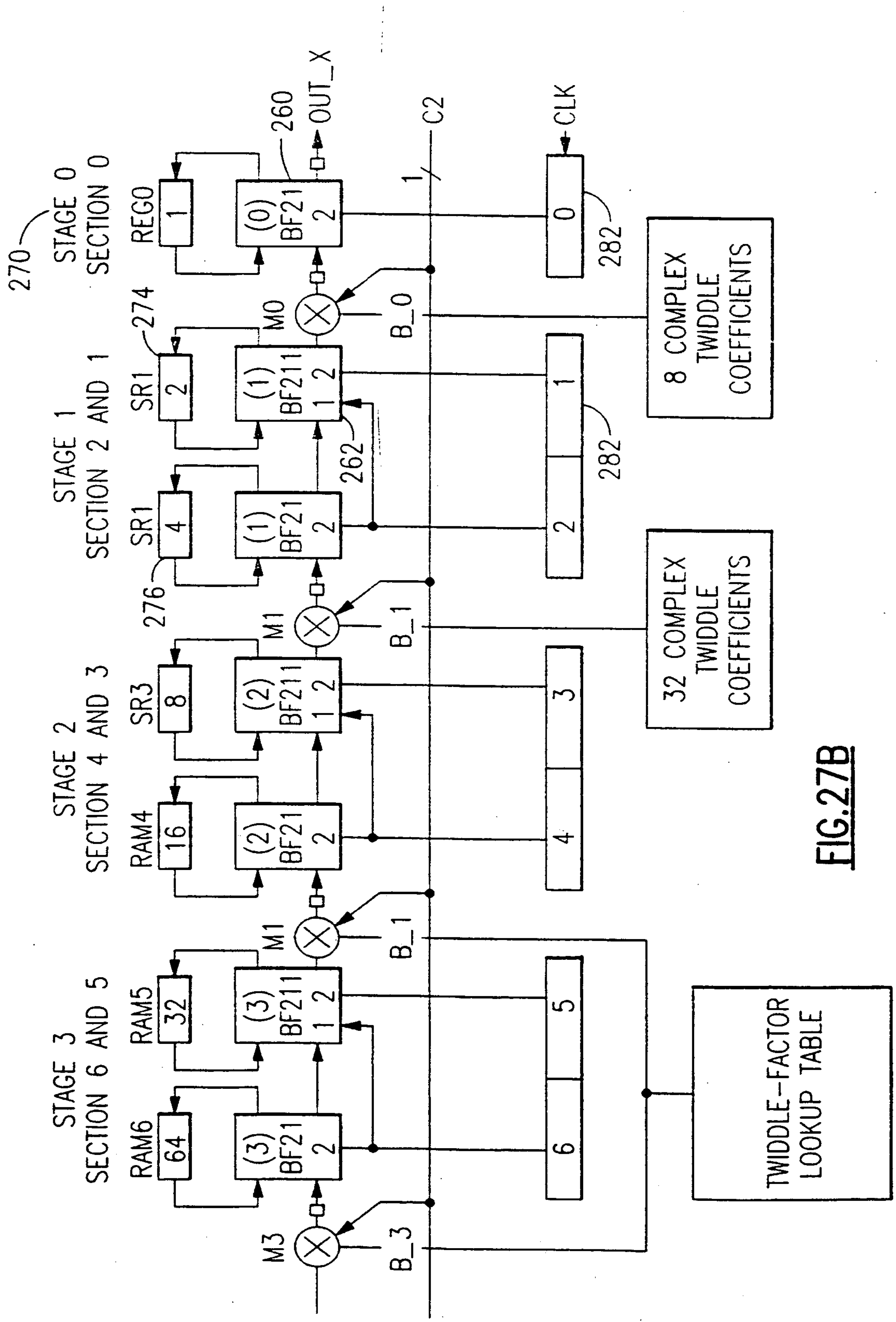

270
STAGE 0
SECTION 0
REG0
1
(0)
BF21
2
260
OUT_X
C2
1
CLK
0
282
274
SR1
2
(1)
BF211
1 2
M0
B_0
8 COMPLEX
TWIDDLE
COEFFICIENTS
STAGE 1
SECTION 2 AND 1
262
282
1
2
SR1
4
(1)
BF21
2
276
M1
B_1
32 COMPLEX
TWIDDLE
COEFFICIENTS
STAGE 2
SECTION 4 AND 3
SR3
8
(2)
BF211
1 2
3
RAM4
16
(2)
BF21
2
4
M1
B_1
STAGE 3
SECTION 6 AND 5
RAM5
32
(3)
BF211
1 2
5
RAM6
64
(3)
BF21
2
6
M3
B_3
TWIDDLE-FACTOR
LOOKUP TABLE

FIG.27B

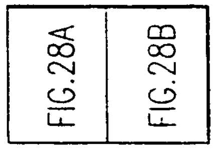


FIG.28

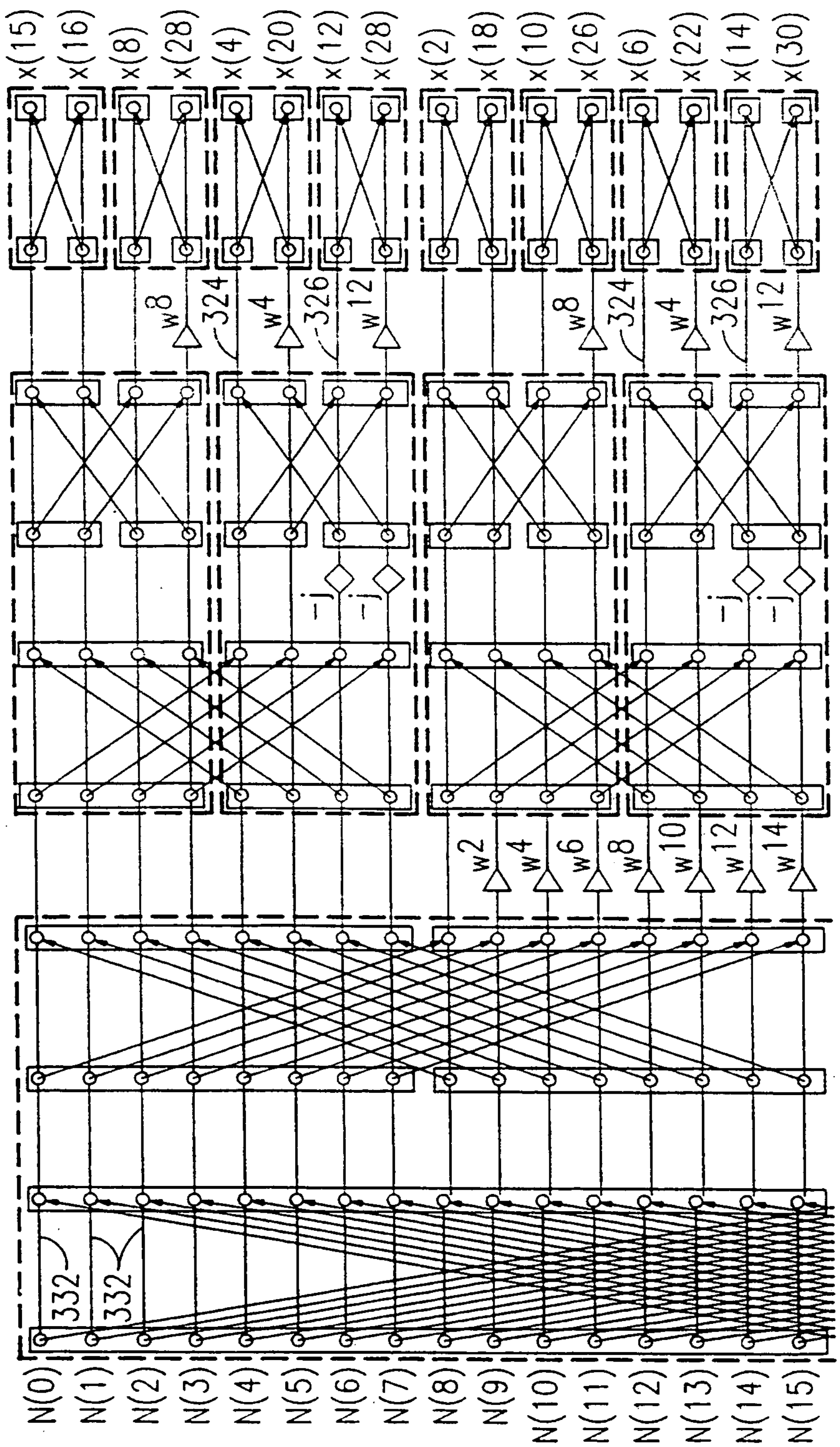
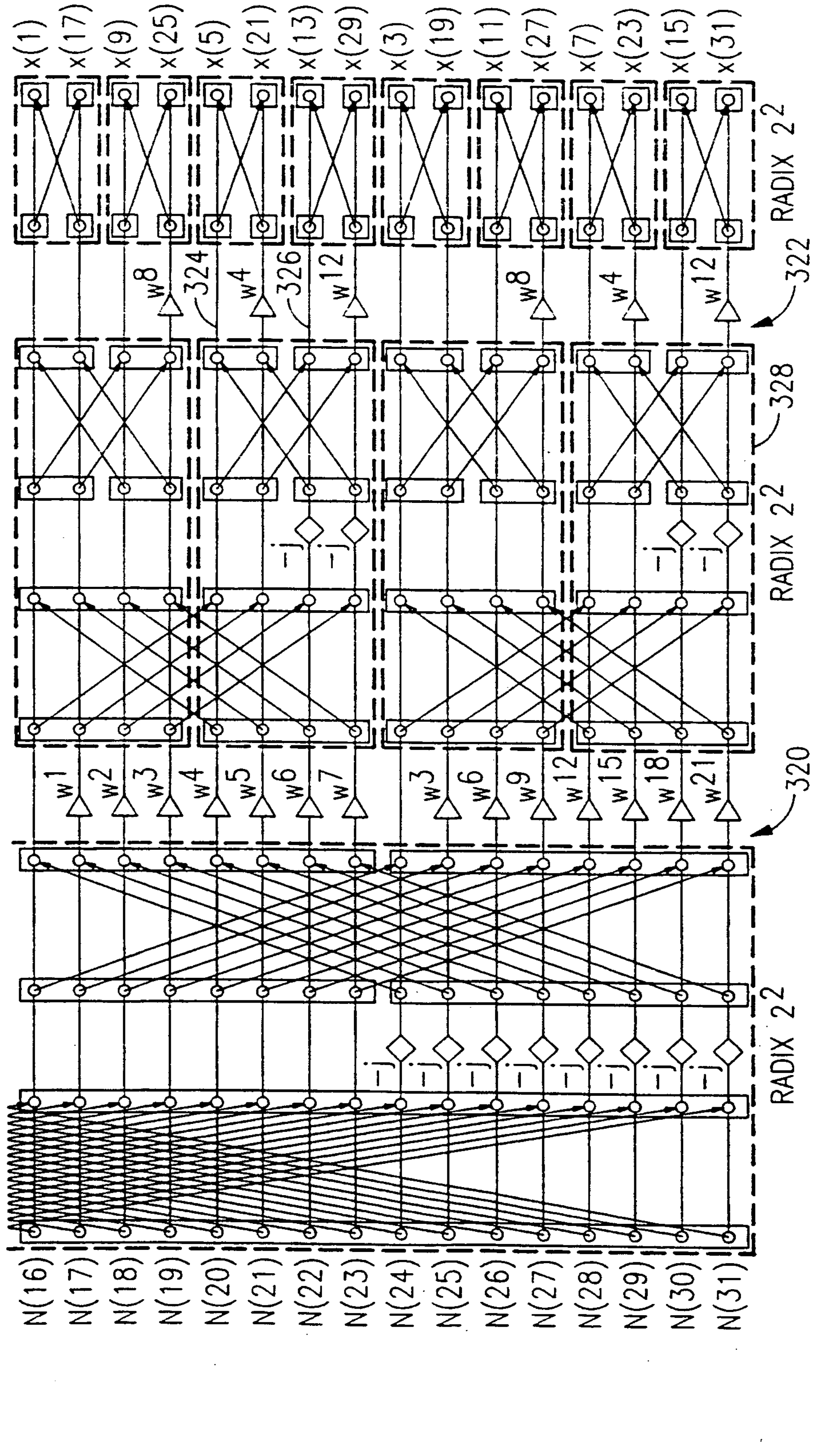


FIG.28A

FIG.28B


x(1)
x(17)
x(9)
x(25)
x(5)
x(21)
x(13)
x(29)
x(3)
x(19)
x(11)
x(27)
x(7)
x(23)
x(15)
x(31)
RADIX 2^2
322
324
326
328
w^8
w^4
w^12
-j
RADIX 2^2
320
w^1
w^2
w^3
w^4
w^5
w^6
w^7
w^3
w^6
w^9
w^12
w^15
w^18
w^21
RADIX 2^2
N(16)
N(17)
N(18)
N(19)
N(20)
N(21)
N(22)
N(23)
N(24)
N(25)
N(26)
N(27)
N(28)
N(29)
N(30)
N(31)

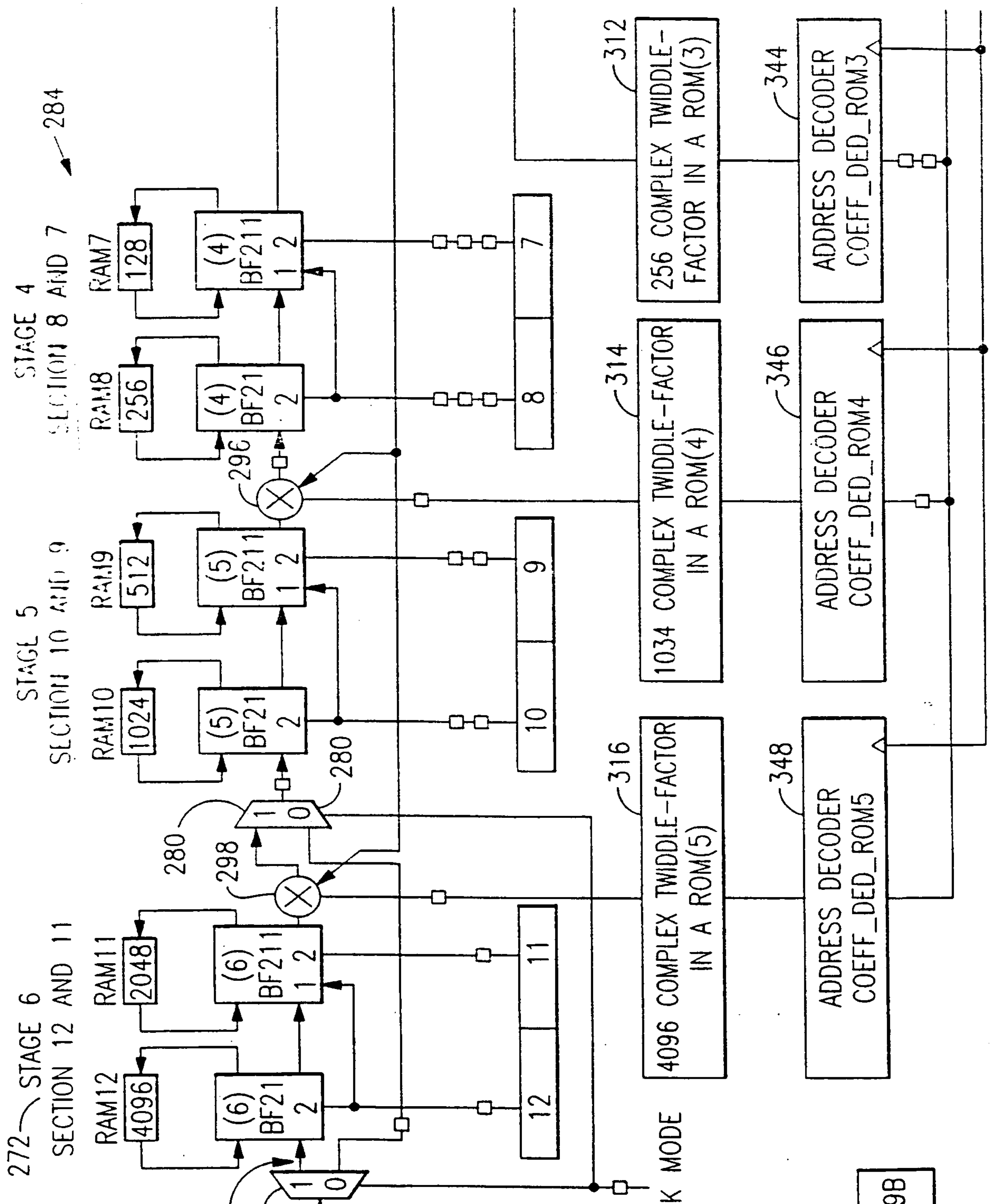


FIG.29A

FIG.29

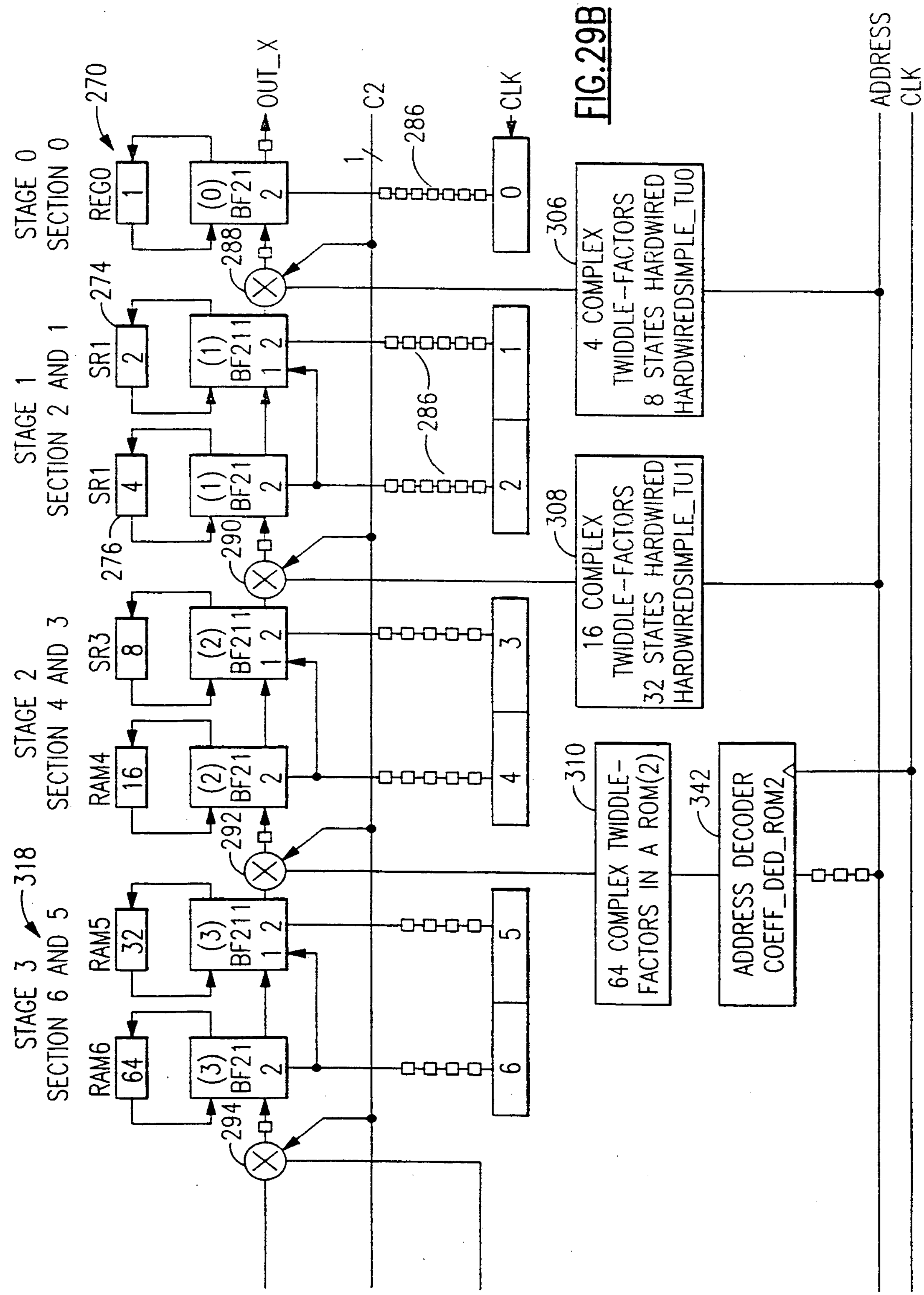

STAGE 0
SECTION 0
270
REG0
1
(0)
BF21
2
OUT_X
288
STAGE 1
SECTION 2 AND 1
274
SR1
2
(1)
BF211
1 2
SR1
4
(1)
BF21
2
276
290
STAGE 2
SECTION 4 AND 3
SR3
8
(2)
BF211
1 2
RAM4
16
(2)
BF21
2
292
STAGE 3
SECTION 6 AND 5
318
RAM5
32
(3)
BF211
1 2
RAM6
64
(3)
BF21
2
294
C2
1
286
CLK
0
1
2
3
4
5
6
306
4 COMPLEX
TWIDDLE-FACTORS
8 STATES HARDWIRED
HARDWIREDSIMPLE_TU0
308
16 COMPLEX
TWIDDLE-FACTORS
32 STATES HARDWIRED
HARDWIREDSIMPLE_TU1
310
64 COMPLEX TWIDDLE-
FACTORS IN A ROM(2)
342
ADDRESS DECODER
COEFF_DED_ROM2
ADDRESS
CLK

FIG.29B

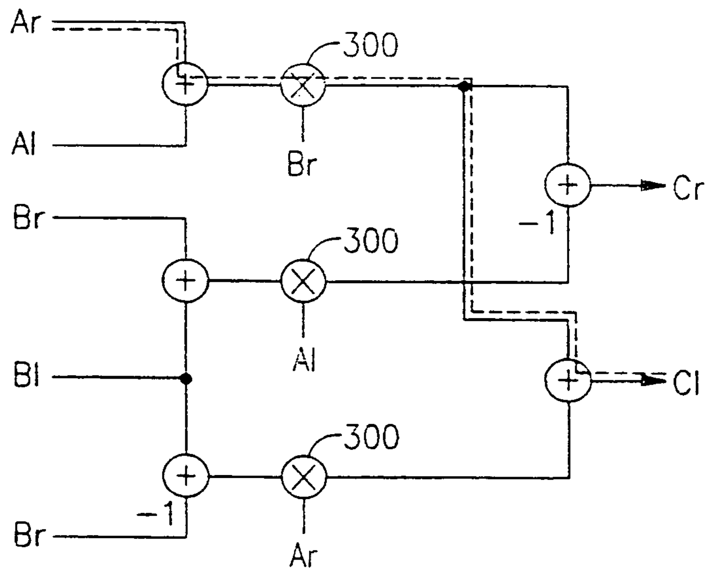

Ar
300
Al
Br
Cr
-1
Br
300
Bl
Al
Cl
300
-1
Br
Ar

FIG.30

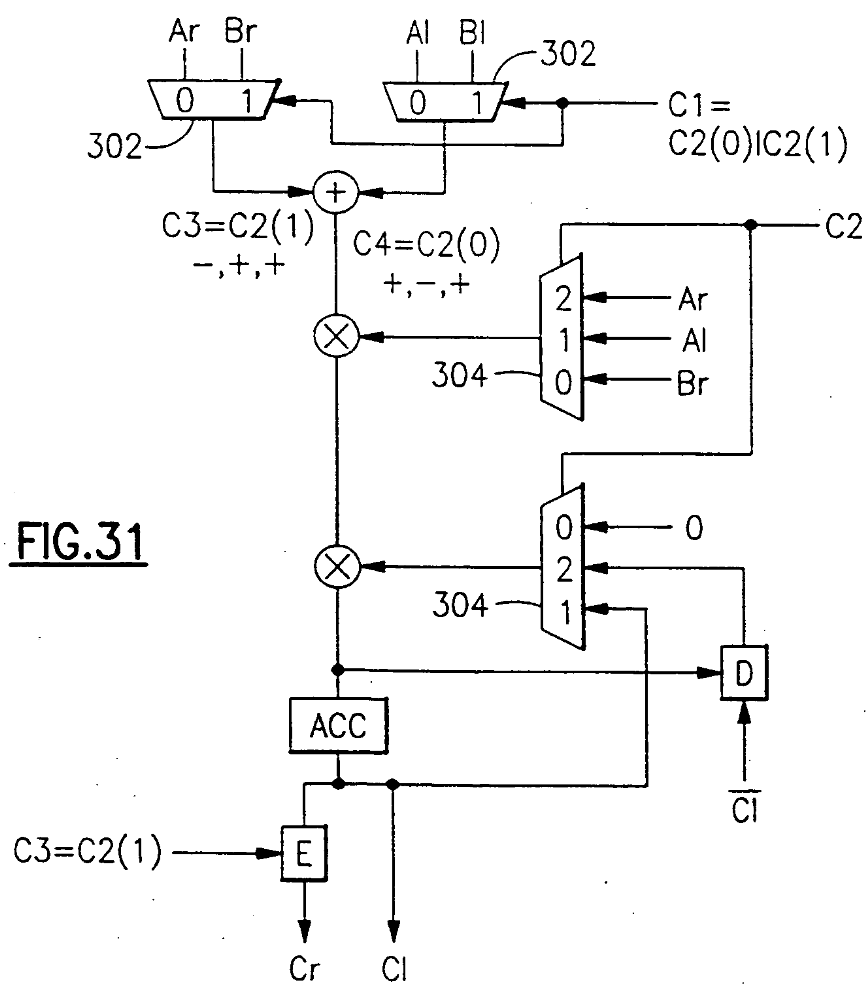

Ar Br
Al Bl
302
0 1
0 1
302
C1=
C2(0)lC2(1)
C3=C2(1)
-,+,+
C4=C2(0)
+,-,+
C2
2 Ar
1 Al
304 0 Br
0 0
2
304 1
D
ACC
Cl
C3=C2(1)
E
Cr Cl

FIG.31

MULTIPLIER M3

330

w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}
w^{0}	w^{2}	w^{4}	w^{6}	w^{8}	w^{10}	w^{12}	w^{14}	w^{16}	w^{18}	w^{20}	w^{22}	w^{24}	w^{26}	w^{28}	w^{30}
w^{0}	w^{1}	w^{2}	w^{3}	w^{4}	w^{5}	w^{6}	w^{7}	w^{8}	w^{9}	w^{10}	w^{11}	w^{12}	w^{13}	w^{14}	w^{15}
w^{0}	w^{3}	w^{6}	w^{9}	w^{12}	w^{15}	w^{18}	w^{21}	w^{24}	w^{27}	w^{30}	w^{33}	w^{36}	w^{39}	w^{42}	w^{45}

w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}
w^{64}	w^{66}	w^{68}	w^{70}	w^{72}	w^{74}	w^{76}	w^{78}	w^{80}	w^{82}	w^{84}	w^{86}	w^{88}	w^{90}	w^{92}	w^{94}
w^{32}	w^{33}	w^{34}	w^{35}	w^{36}	w^{37}	w^{38}	w^{39}	w^{40}	w^{41}	w^{42}	w^{43}	w^{44}	w^{45}	w^{46}	w^{47}
w^{96}	w^{99}	w^{102}	w^{105}	w^{108}	w^{111}	w^{114}	w^{117}	w^{120}	w^{123}	w^{126}	w^{129}	w^{132}	w^{135}	w^{138}	w^{141}

w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}
w^{128}	w^{130}	w^{132}	w^{134}	w^{136}	w^{138}	w^{140}	w^{142}	w^{144}	w^{146}	w^{148}	w^{150}	w^{152}	w^{154}	w^{156}	w^{158}
w^{64}	w^{65}	w^{66}	w^{67}	w^{68}	w^{69}	w^{70}	w^{71}	w^{72}	w^{73}	w^{74}	w^{75}	w^{76}	w^{77}	w^{78}	w^{79}
w^{192}	w^{195}	w^{198}	w^{201}	w^{204}	w^{207}	w^{210}	w^{213}	w^{216}	w^{219}	w^{222}	w^{225}	w^{228}	w^{231}	w^{234}	w^{237}

w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}
w^{192}	w^{194}	w^{196}	w^{198}	w^{200}	w^{202}	w^{204}	w^{206}	w^{208}	w^{210}	w^{212}	w^{214}	w^{216}	w^{218}	w^{220}	w^{222}
w^{96}	w^{97}	w^{98}	w^{99}	w^{100}	w^{101}	w^{102}	w^{103}	w^{104}	w^{105}	w^{106}	w^{107}	w^{108}	w^{109}	w^{110}	w^{111}
w^{288}	w^{291}	w^{294}	w^{297}	w^{300}	w^{303}	w^{306}	w^{309}	w^{312}	w^{315}	w^{318}	w^{321}	w^{324}	w^{327}	w^{330}	w^{333}

FIG.32A

FIG.32A	FIG.32B

FIG.32

w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}
w^{32}	w^{34}	w^{36}	w^{38}	w^{40}	w^{42}	w^{44}	w^{46}	w^{48}	w^{50}	w^{52}	w^{54}	w^{56}	w^{58}	w^{60}	w^{62}
w^{16}	w^{17}	w^{18}	w^{19}	w^{20}	w^{21}	w^{22}	w^{23}	w^{24}	w^{25}	w^{26}	w^{27}	w^{28}	w^{29}	w^{30}	w^{31}
w^{48}	w^{51}	w^{54}	w^{57}	w^{60}	w^{63}	w^{66}	w^{69}	w^{72}	w^{75}	w^{78}	w^{81}	w^{84}	w^{87}	w^{90}	w^{93}

w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}
w^{96}	w^{98}	w^{100}	w^{102}	w^{104}	w^{106}	w^{108}	w^{110}	w^{112}	w^{114}	w^{116}	w^{118}	w^{120}	w^{122}	w^{124}	w^{126}
w^{48}	w^{49}	w^{50}	w^{51}	w^{52}	w^{53}	w^{54}	w^{55}	w^{56}	w^{57}	w^{58}	w^{59}	w^{60}	w^{61}	w^{62}	w^{63}
w^{144}	w^{147}	w^{150}	w^{153}	w^{156}	w^{159}	w^{162}	w^{165}	w^{168}	w^{171}	w^{174}	w^{177}	w^{180}	w^{183}	w^{186}	w^{189}

w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}
w^{160}	w^{162}	w^{164}	w^{166}	w^{168}	w^{170}	w^{172}	w^{174}	w^{176}	w^{178}	w^{180}	w^{182}	w^{184}	w^{186}	w^{188}	w^{190}
w^{80}	w^{81}	w^{82}	w^{83}	w^{84}	w^{85}	w^{86}	w^{87}	w^{88}	w^{89}	w^{90}	w^{91}	w^{92}	w^{93}	w^{94}	w^{95}
w^{240}	w^{243}	w^{246}	w^{249}	w^{252}	w^{255}	w^{258}	w^{261}	w^{264}	w^{267}	w^{270}	w^{273}	w^{276}	w^{279}	w^{282}	w^{285}

w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}	w^{0}
w^{224}	w^{226}	w^{228}	w^{230}	w^{232}	w^{234}	w^{236}	w^{238}	w^{240}	w^{242}	w^{244}	w^{246}	w^{248}	w^{250}	w^{252}	w^{254}
w^{112}	w^{113}	w^{114}	w^{115}	w^{116}	w^{117}	w^{118}	w^{119}	w^{120}	w^{121}	w^{122}	w^{123}	w^{124}	w^{125}	w^{126}	w^{127}
w^{336}	w^{339}	w^{342}	w^{345}	w^{348}	w^{351}	w^{354}	w^{357}	w^{360}	w^{363}	w^{366}	w^{369}	w^{372}	w^{375}	w^{378}	w^{381}

FIG.32B

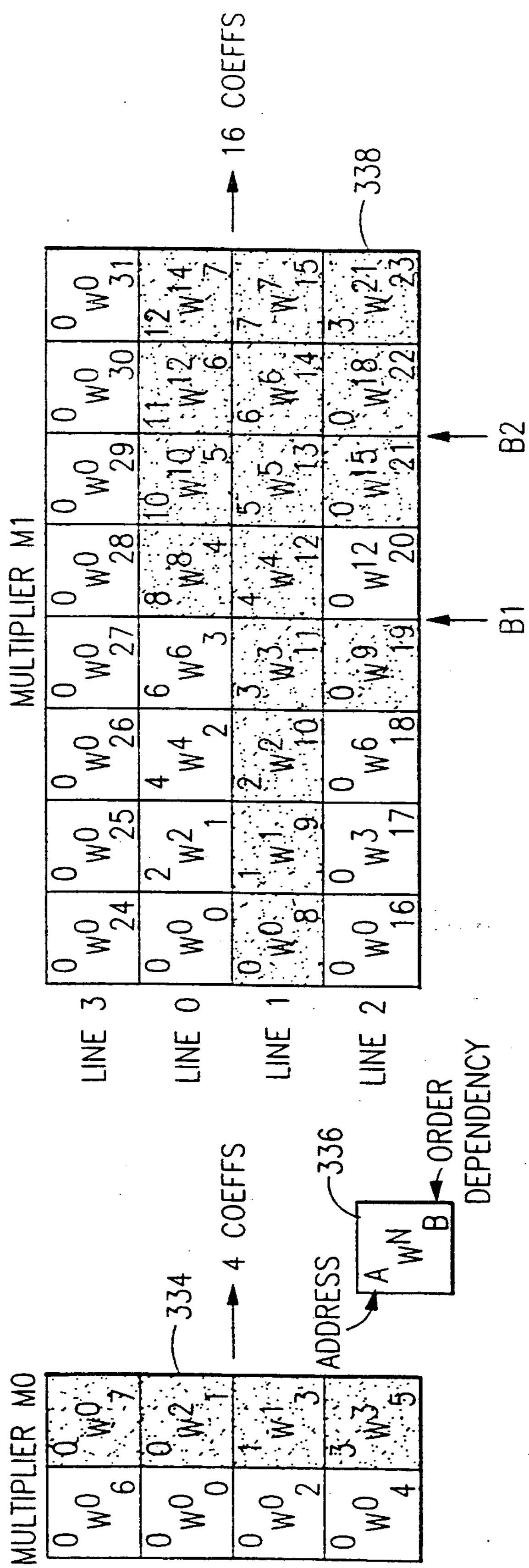

MULTIPLIER M1
16 COEFFS
338
LINE 3
LINE 0
LINE 1
LINE 2
B1
B2
MULTIPLIER M0
4 COEFFS
334
ADDRESS
336
ORDER DEPENDENCY

FIG.33A

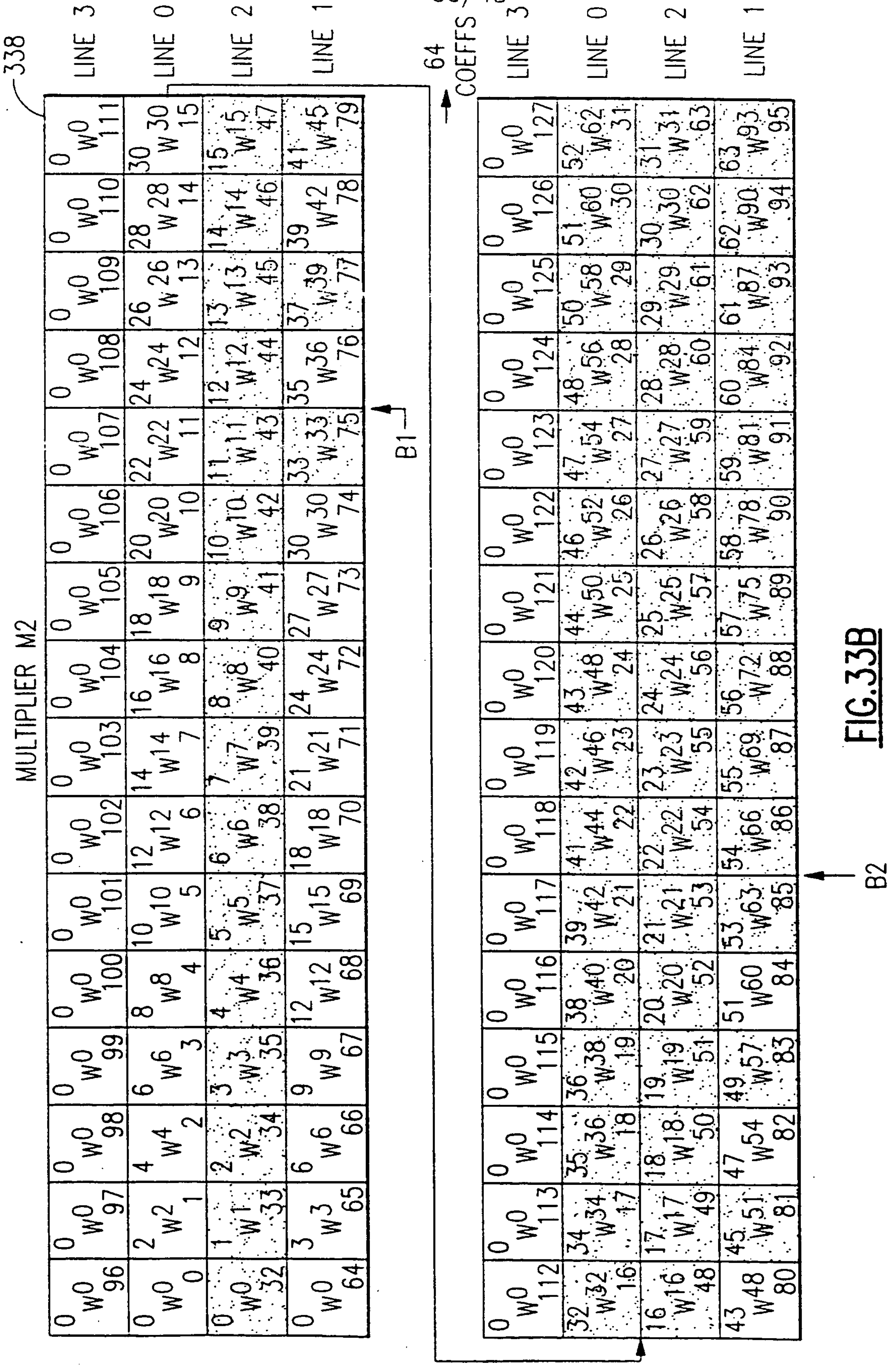


FIG.33B

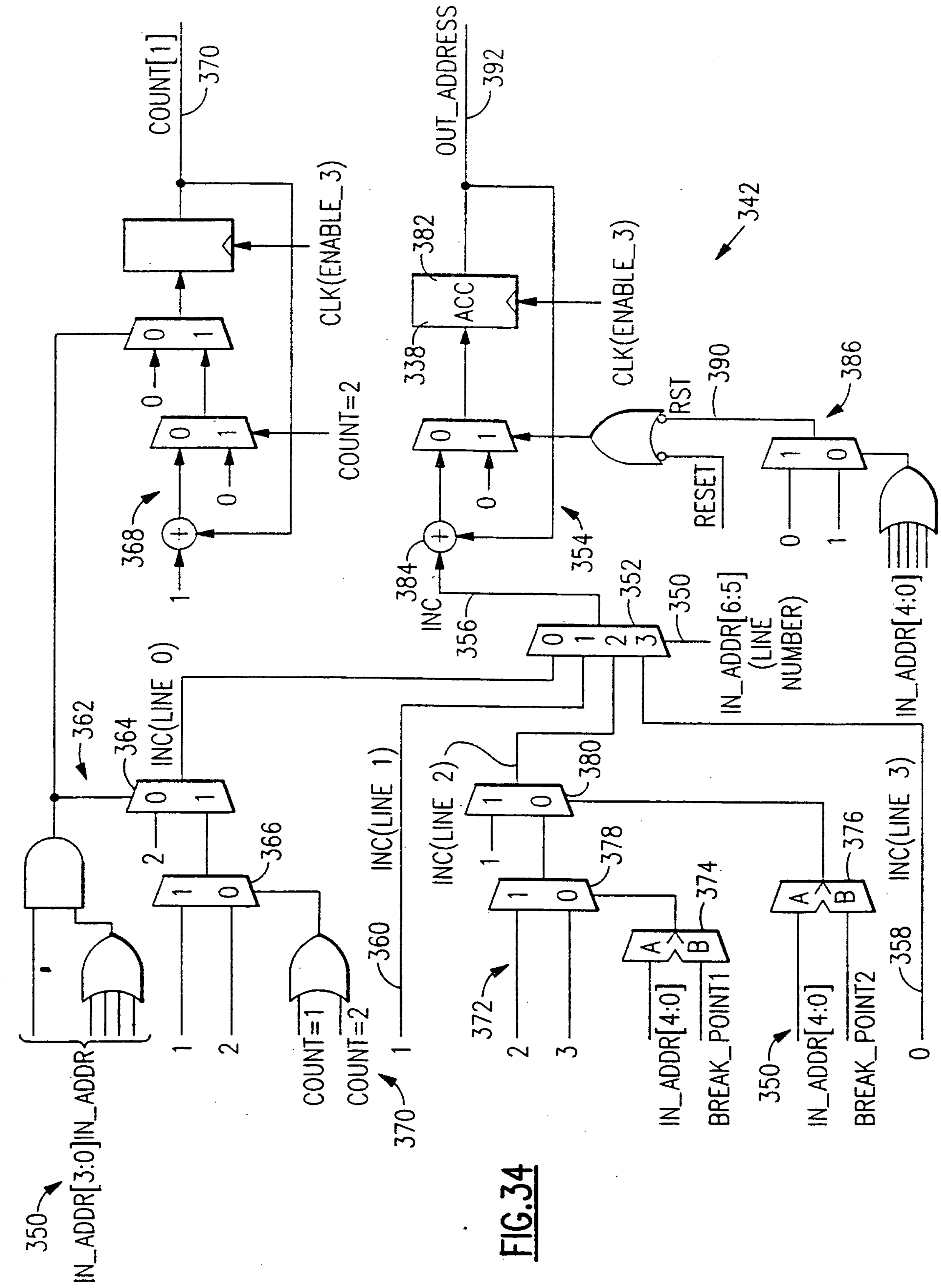

COUNT[1]
370
OUT_ADDRESS
392
382
ACC
338
CLK(ENABLE_3)
CLK(ENABLE_3)
342
COUNT=2
368
RST
390
RESET
386
354
384
INC
356
352
350
IN_ADDR[6:5]
(LINE
NUMBER)
IN_ADDR[4:0]
362
364
INC(LINE 0)
INC(LINE 1)
INC(LINE 2)
380
378
376
374
366
360
372
358
INC(LINE 3)
350
IN_ADDR[3:0]
IN_ADDR
COUNT=1
COUNT=2
370
IN_ADDR[4:0]
BREAK_POINT1
IN_ADDR[4:0]
BREAK_POINT2

FIG.34

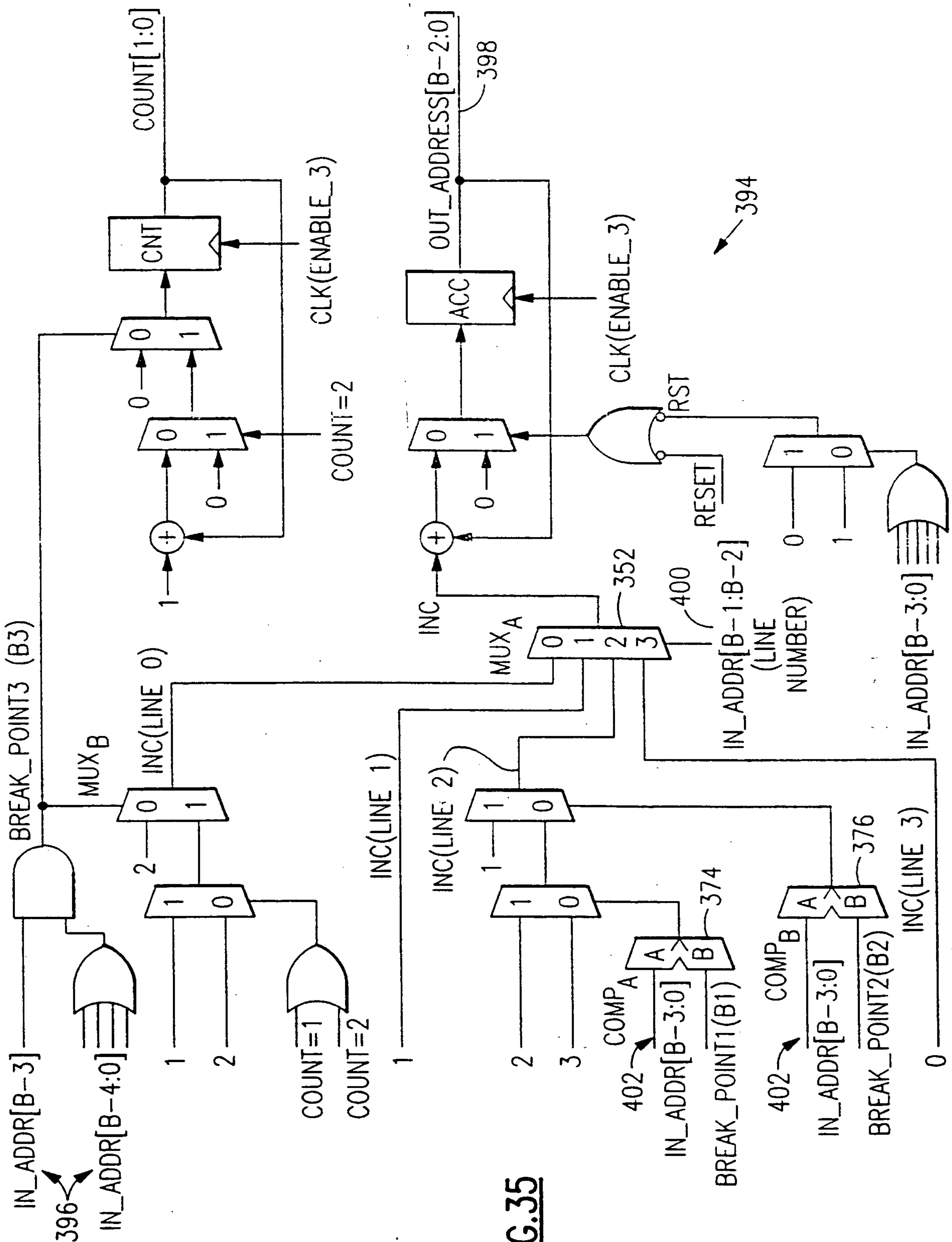

COUNT[1:0]
CNT
CLK(ENABLE_3)
COUNT=2
OUT_ADDRESS[B-2:0]
398
ACC
CLK(ENABLE_3)
RST
RESET
394
BREAK_POINT3 (B3)
MUX_B
INC(LINE 0)
INC
352
MUX_A
400
IN_ADDR[B-1:B-2]
(LINE
NUMBER)
IN_ADDR[B-3:0]
INC(LINE 1)
INC(LINE 2)
376
374
COMP_A
COMP_B
INC(LINE 3)
IN_ADDR[B-3]
IN_ADDR[B-4:0]
396
COUNT=1
COUNT=2
402
IN_ADDR[B-3:0]
BREAK_POINT1(B1)
BREAK_POINT2(B2)

FIG.35

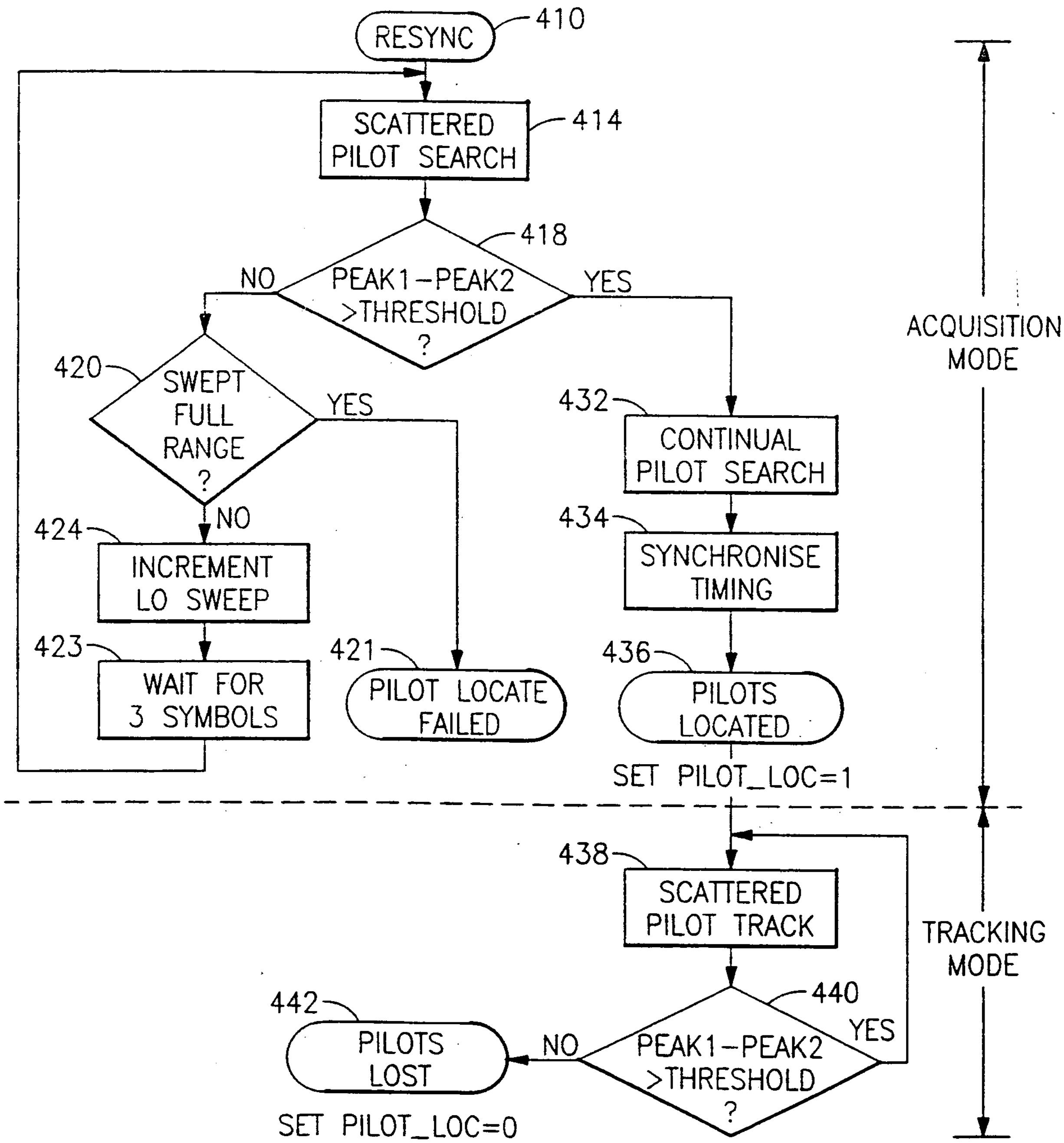

RESYNC
410
SCATTERED PILOT SEARCH
414
418
PEAK1-PEAK2 >THRESHOLD ?
NO
YES
420
SWEPT FULL RANGE ?
YES
NO
424
INCREMENT LO SWEEP
423
WAIT FOR 3 SYMBOLS
421
PILOT LOCATE FAILED
432
CONTINUAL PILOT SEARCH
434
SYNCHRONISE TIMING
436
PILOTS LOCATED
SET PILOT_LOC=1
ACQUISITION MODE
438
SCATTERED PILOT TRACK
440
PEAK1-PEAK2 >THRESHOLD ?
YES
NO
442
PILOTS LOST
SET PILOT_LOC=0
TRACKING MODE

FIG.36

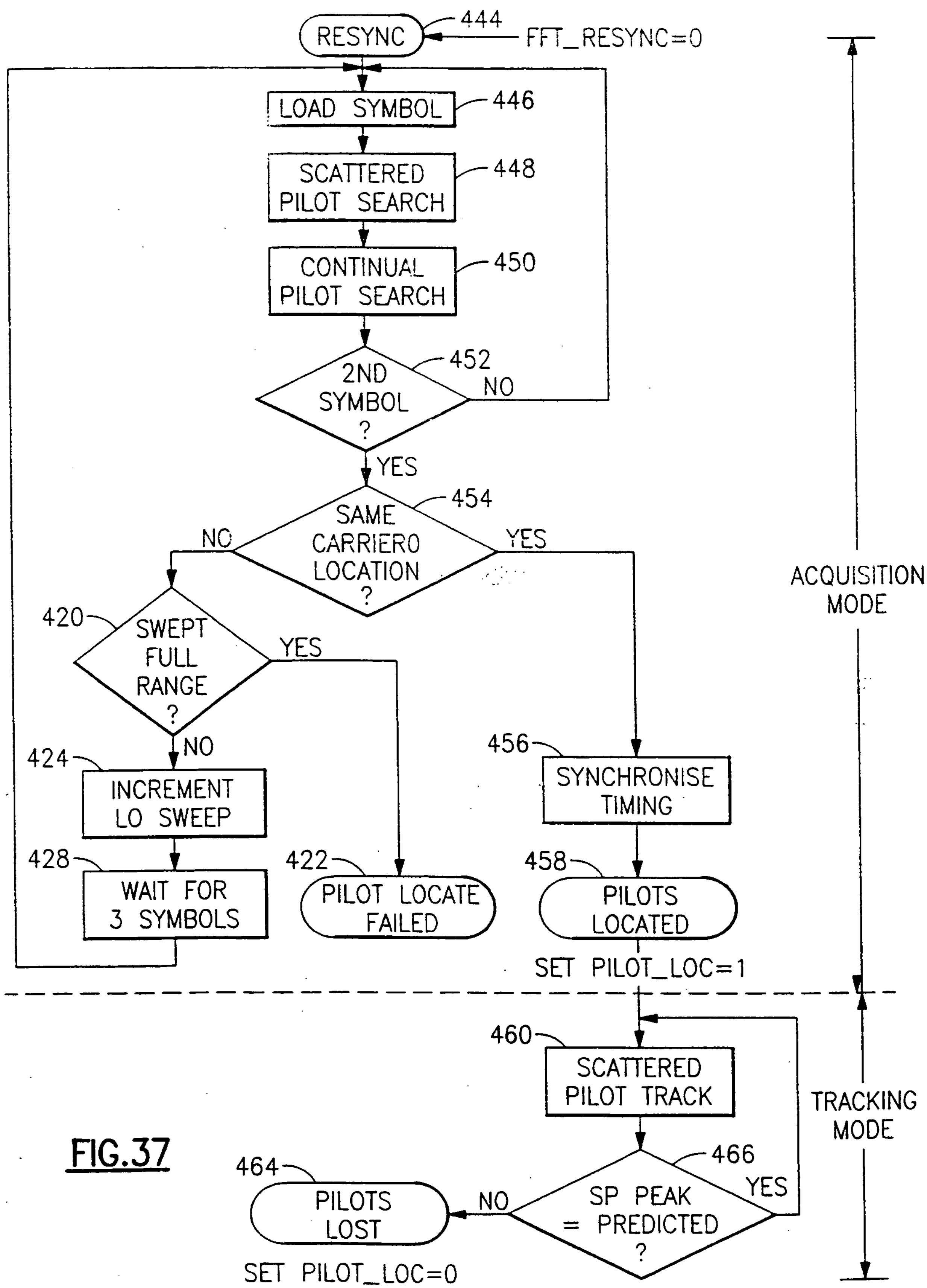

RESYNC
444
FFT_RESYNC=0
LOAD SYMBOL
446
SCATTERED PILOT SEARCH
448
CONTINUAL PILOT SEARCH
450
2ND SYMBOL ?
452
NO
YES
SAME CARRIER0 LOCATION ?
454
NO
YES
420
SWEPT FULL RANGE ?
YES
NO
424
INCREMENT LO SWEEP
428
WAIT FOR 3 SYMBOLS
422
PILOT LOCATE FAILED
456
SYNCHRONISE TIMING
458
PILOTS LOCATED
SET PILOT_LOC=1
ACQUISITION MODE
460
SCATTERED PILOT TRACK
TRACKING MODE
464
PILOTS LOST
SET PILOT_LOC=0
NO
466
SP PEAK = PREDICTED ?
YES

FIG.37

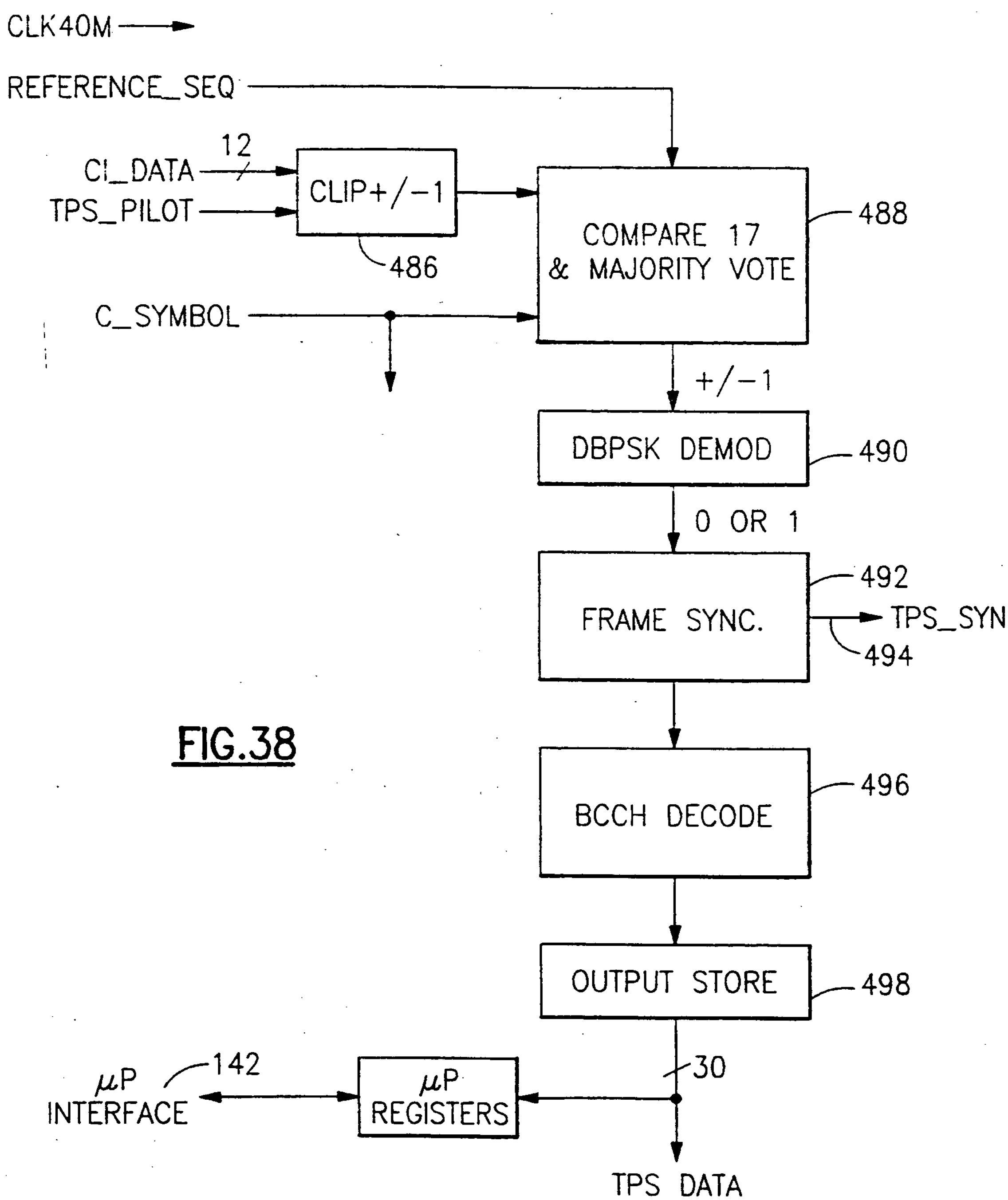

CLK40M
REFERENCE_SEQ
CI_DATA
12
TPS_PILOT
CLIP+/-1
486
COMPARE 17
& MAJORITY VOTE
488
C_SYMBOL
+/-1
DBPSK DEMOD
490
0 OR 1
FRAME SYNC.
492
TPS_SYN
494
BCCH DECODE
496
OUTPUT STORE
498
30
μP
INTERFACE
142
μP
REGISTERS
TPS DATA

FIG.38

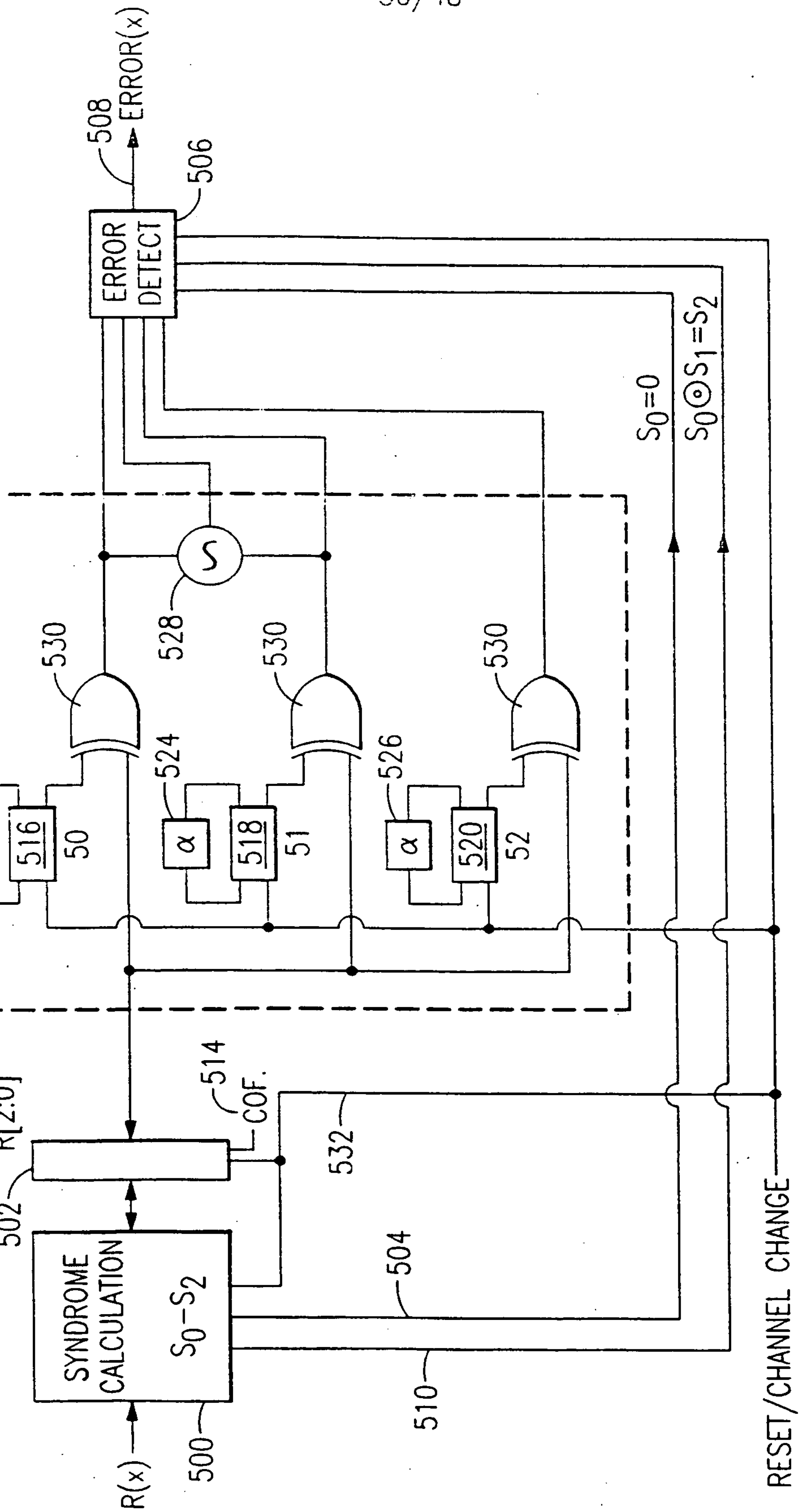

ERROR(x)
508
506
ERROR DETECT
512
528
530
530
530
522
524
526
α
α
α
516
518
520
50
51
52
$S_0=0$
$S_0 \odot S_1=S_2$
R[2:0]
514
COF.
502
532
504
510
SYNDROME CALCULATION
S_0-S_2
500
R(x)
RESET/CHANNEL CHANGE

FIG.39

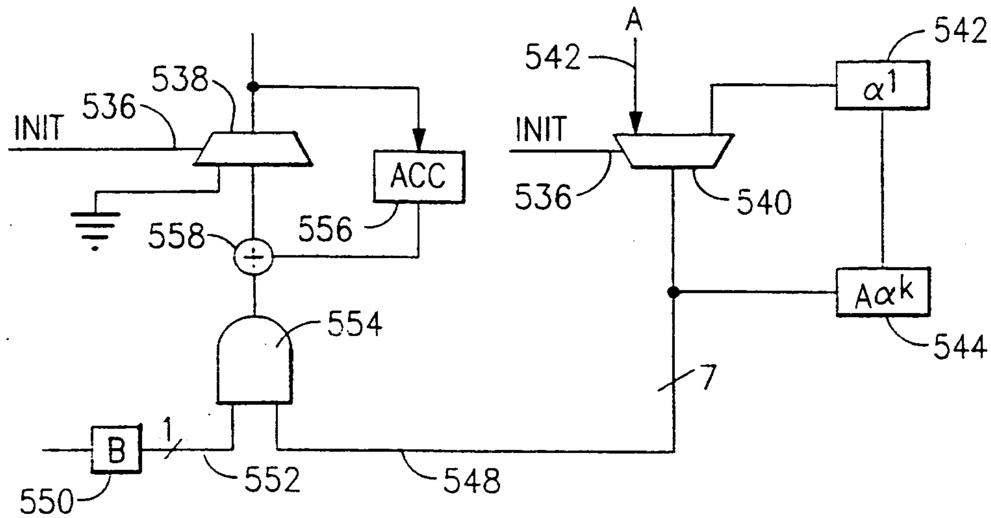

A
542
542
538
536
INIT
INIT
ACC
536
540
558
556
554
$A\alpha^k$
544
7
B
1
550
552
548

FIG.40

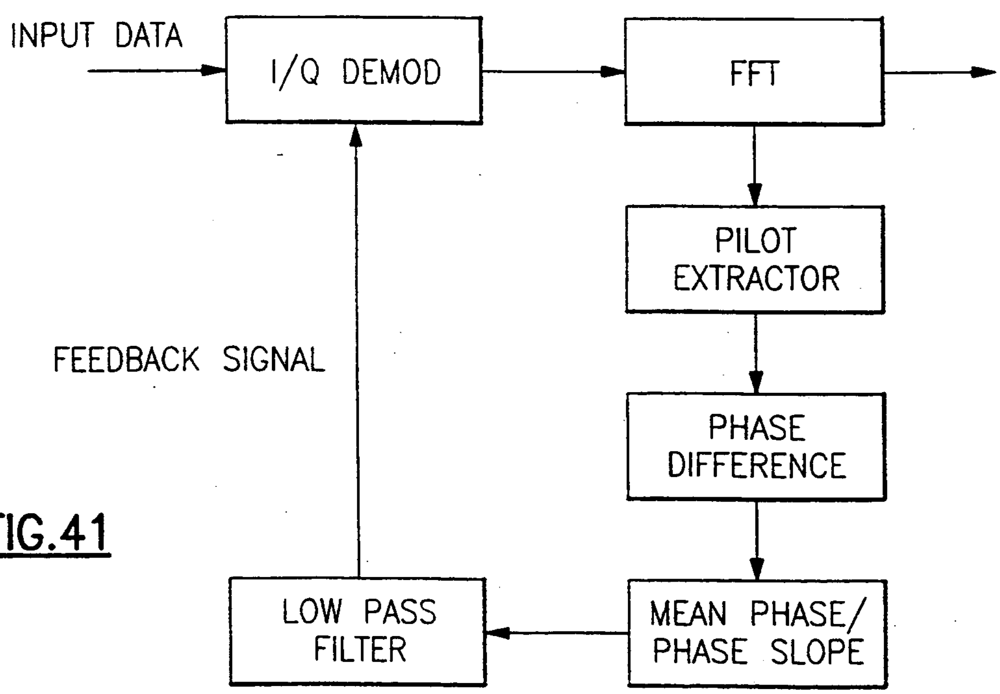
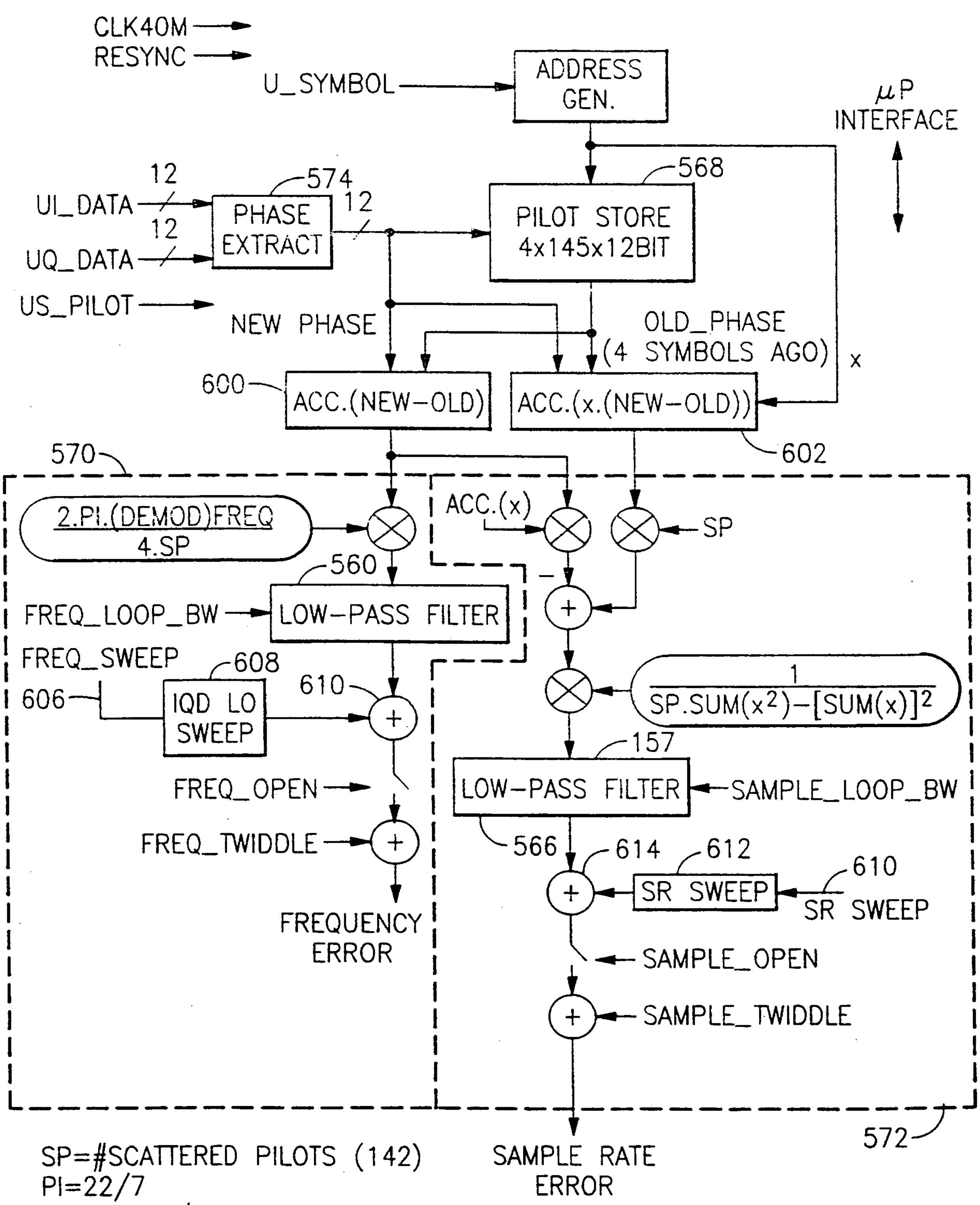

INPUT DATA
I/Q DEMOD
FFT
PILOT EXTRACTOR
FEEDBACK SIGNAL
PHASE DIFFERENCE
LOW PASS FILTER
MEAN PHASE/ PHASE SLOPE

FIG.41



SP=#SCATTERED PILOTS (142)
PI=22/7
DEMOD=32/7MHz
ACC.=ACCUMULATION OF SP SAMPLES

FIG.42

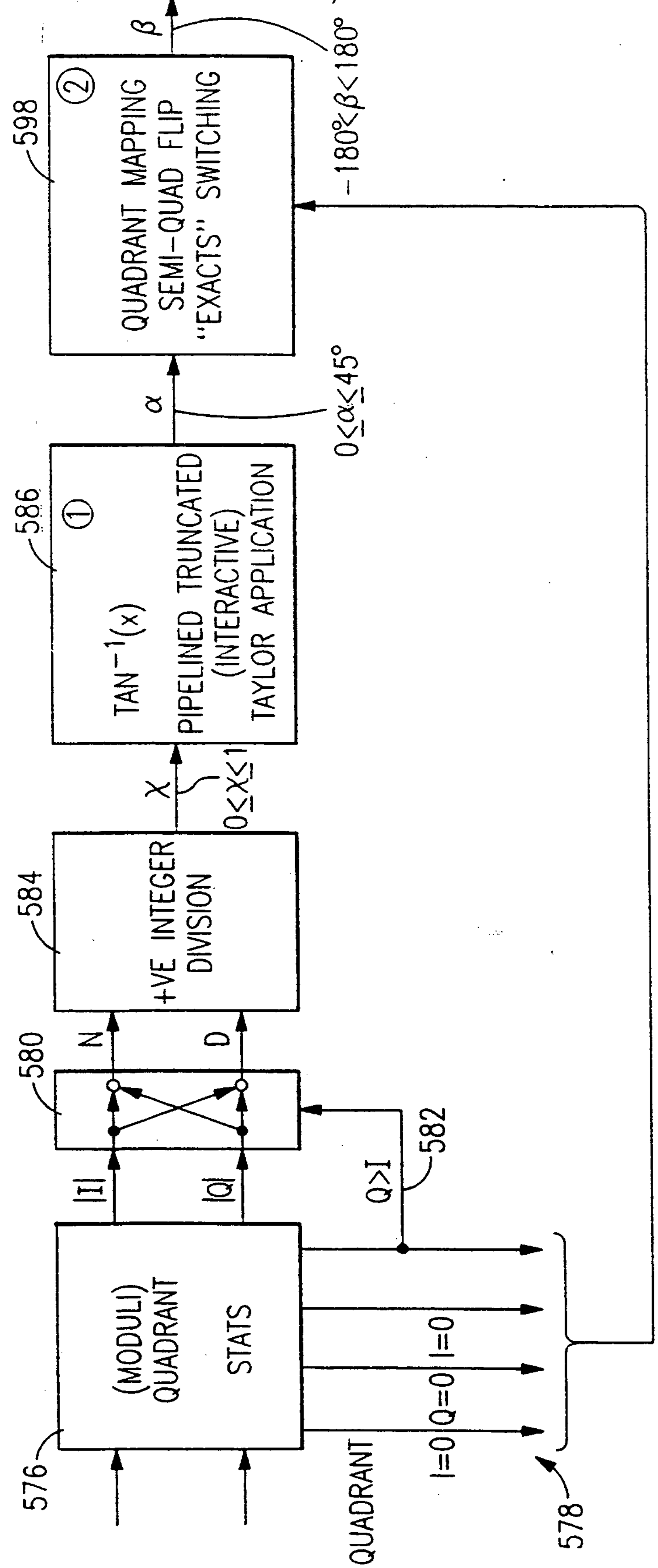

576
(MODULI) QUADRANT STATS
QUADRANT
I=0 Q=0 I=0
578
|I|
|Q|
Q>I
582
580
N
D
584
+VE INTEGER DIVISION
X
0≤X≤1
586
①
TAN⁻¹(x)
PIPELINED TRUNCATED (INTERACTIVE) TAYLOR APPLICATION
α
0≤α≤45°
598
②
QUADRANT MAPPING SEMI-QUAD FLIP "EXACTS" SWITCHING
β
-180°≤β<180°

FIG.43

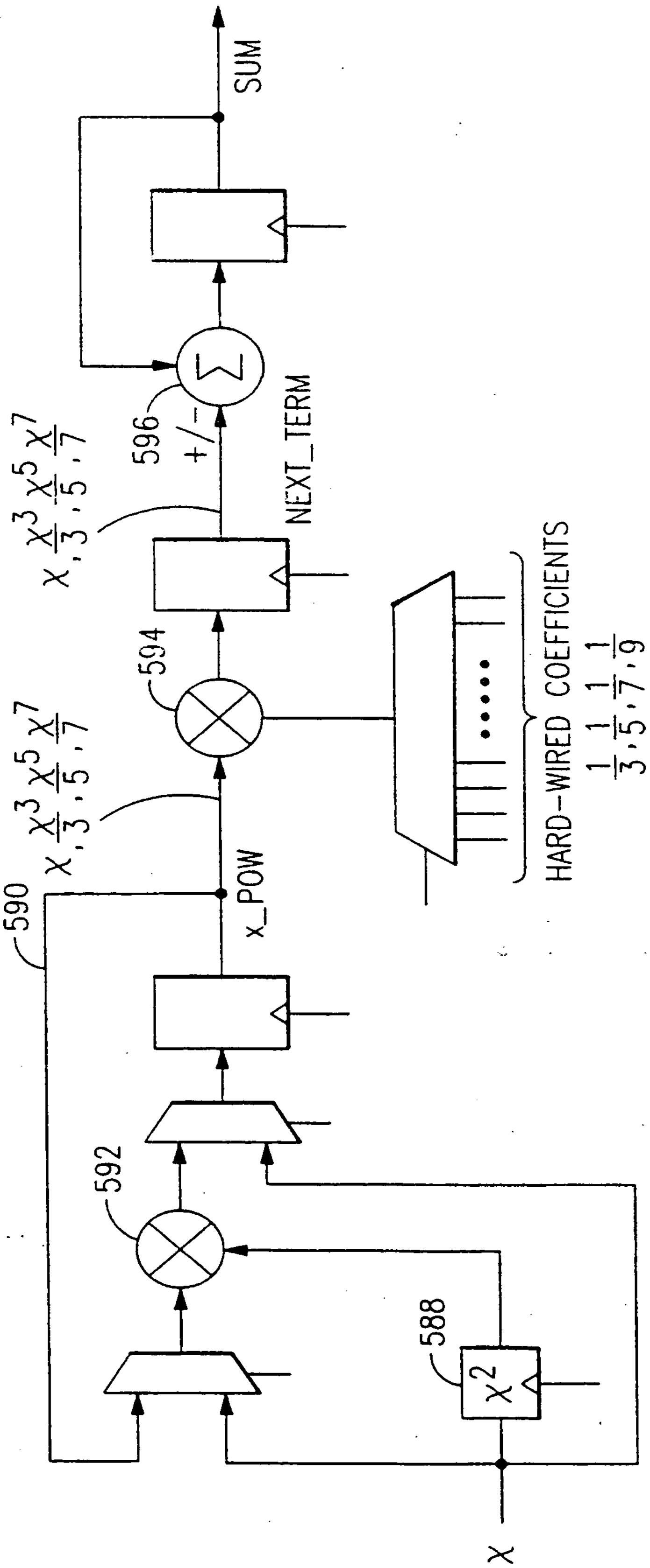

SUM
596
+/-
NEXT_TERM
$X, \frac{X^3}{3}, \frac{X^5}{5}, \frac{X^7}{7}$
594
$X, \frac{X^3}{3}, \frac{X^5}{5}, \frac{X^7}{7}$
590
x_POW
HARD-WIRED COEFFICIENTS
$\frac{1}{3}, \frac{1}{5}, \frac{1}{7}, \frac{1}{9}$
592
588
X^2
X

FIG.44

FIG.45

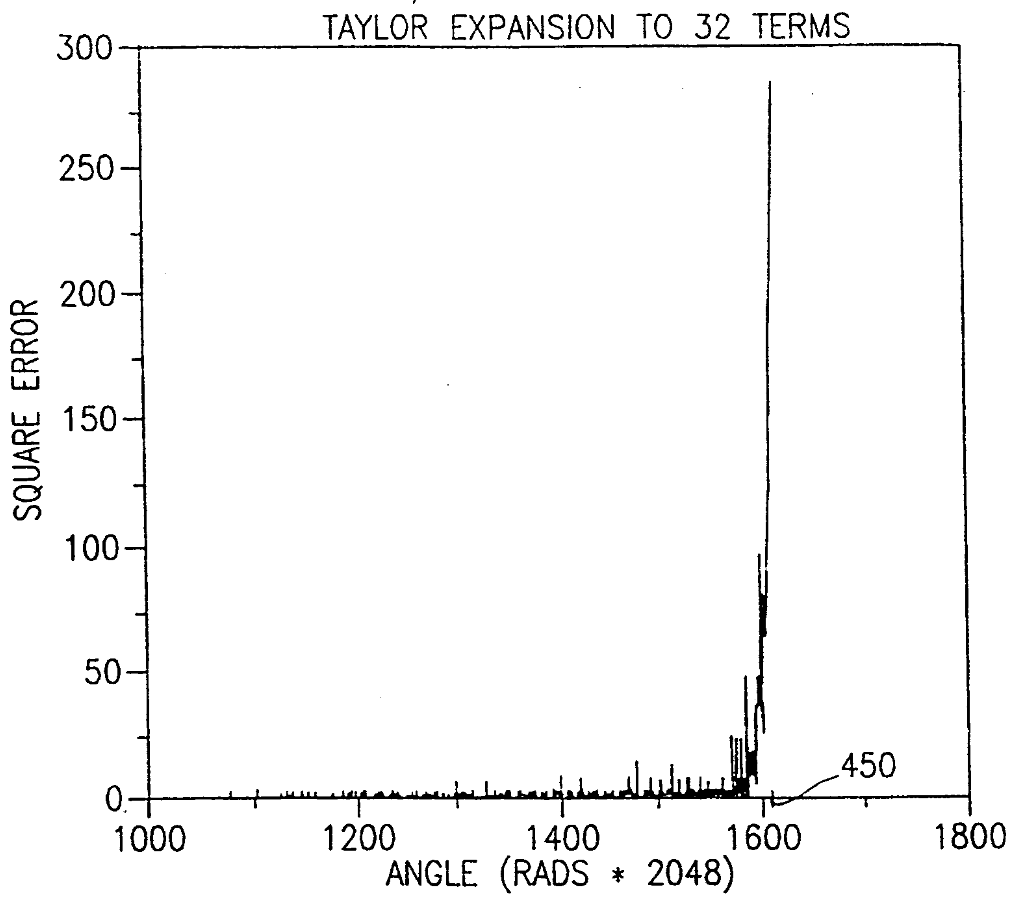
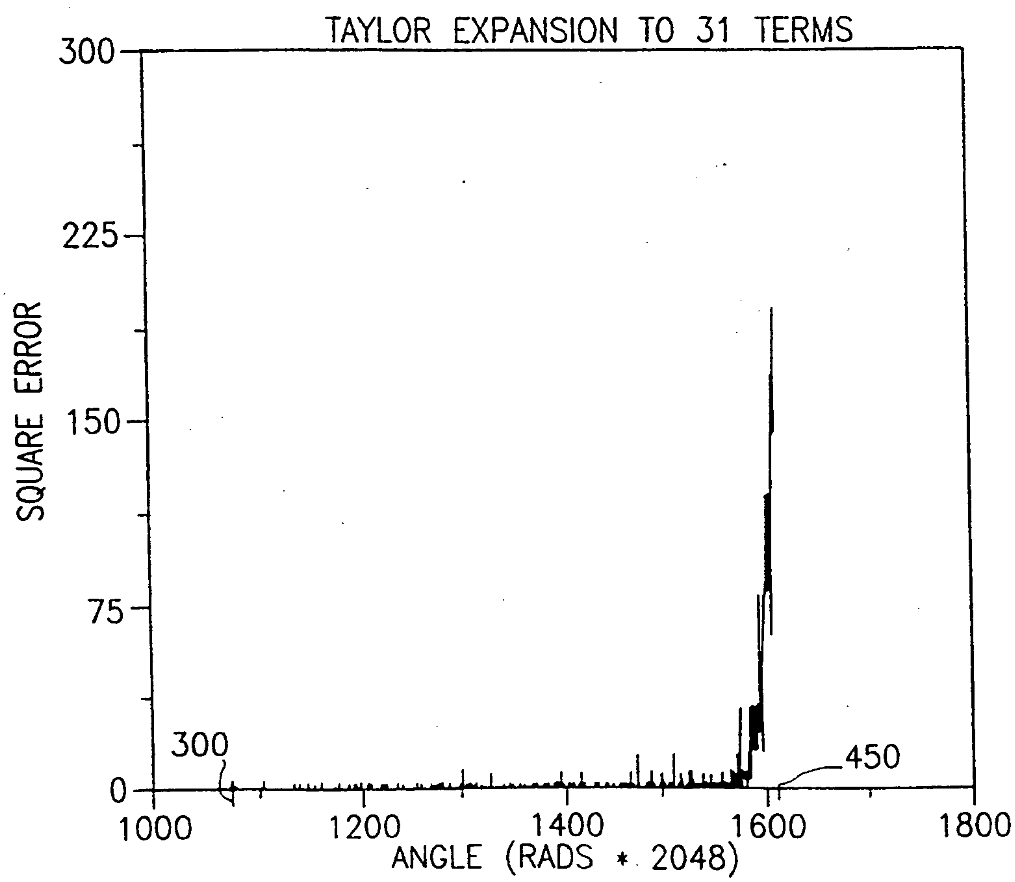

TAYLOR EXPANSION TO 32 TERMS
SQUARE ERROR
300
250
200
150
100
50
0
1000
1200
1400
1600
1800
ANGLE (RADS * 2048)
450

FIG.46


TAYLOR EXPANSION TO 31 TERMS
SQUARE ERROR
300
225
150
75
0
1000
1200
1400
1600
1800
ANGLE (RADS * 2048)
300
450

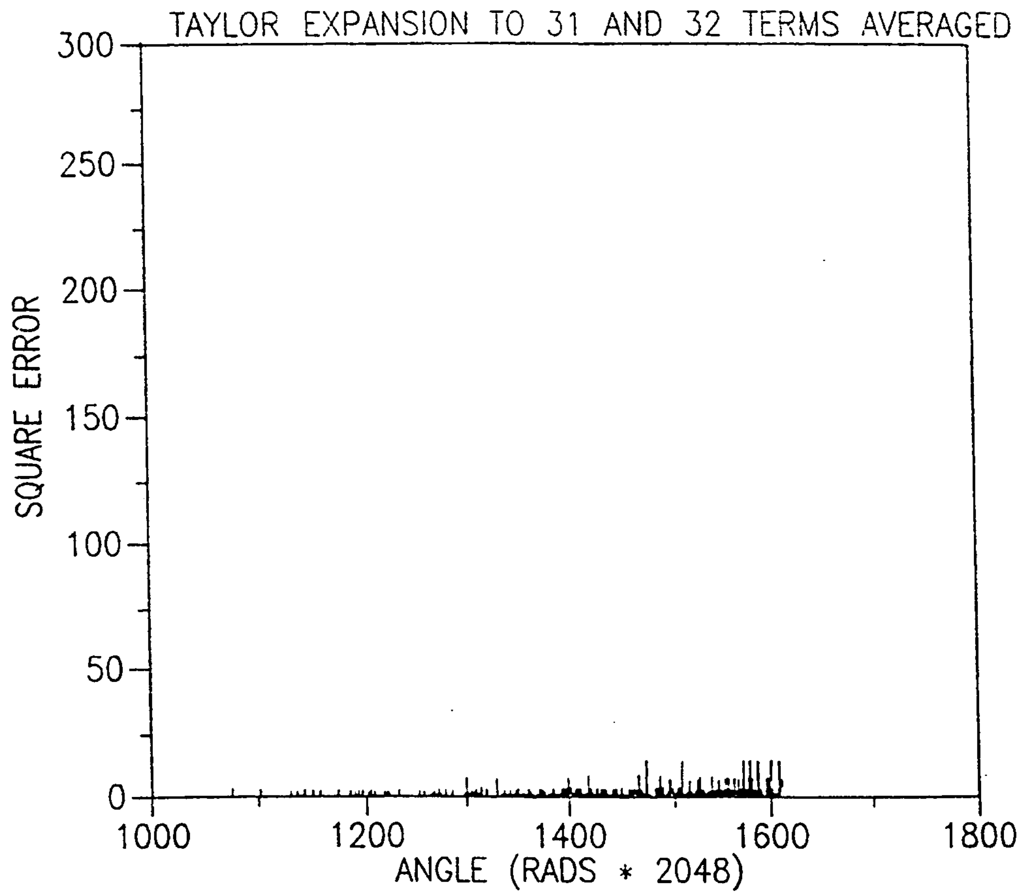

TAYLOR EXPANSION TO 31 AND 32 TERMS AVERAGED
300
250
200
150
100
50
0
SQUARE ERROR
1000
1200
1400
1600
1800
ANGLE (RADS * 2048)

FIG.47

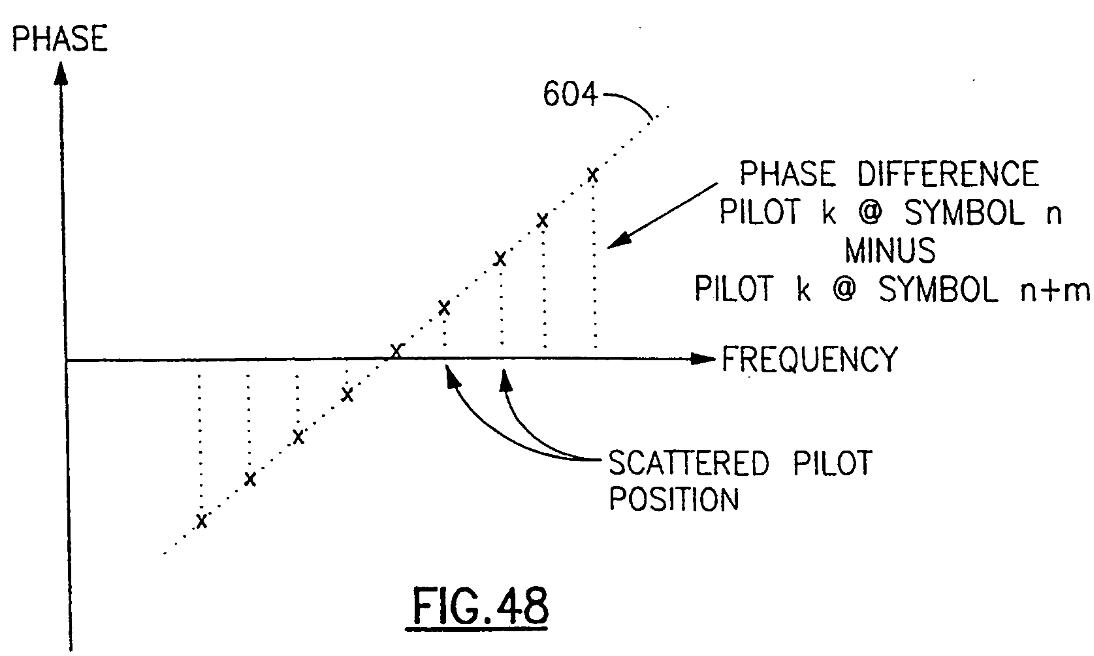
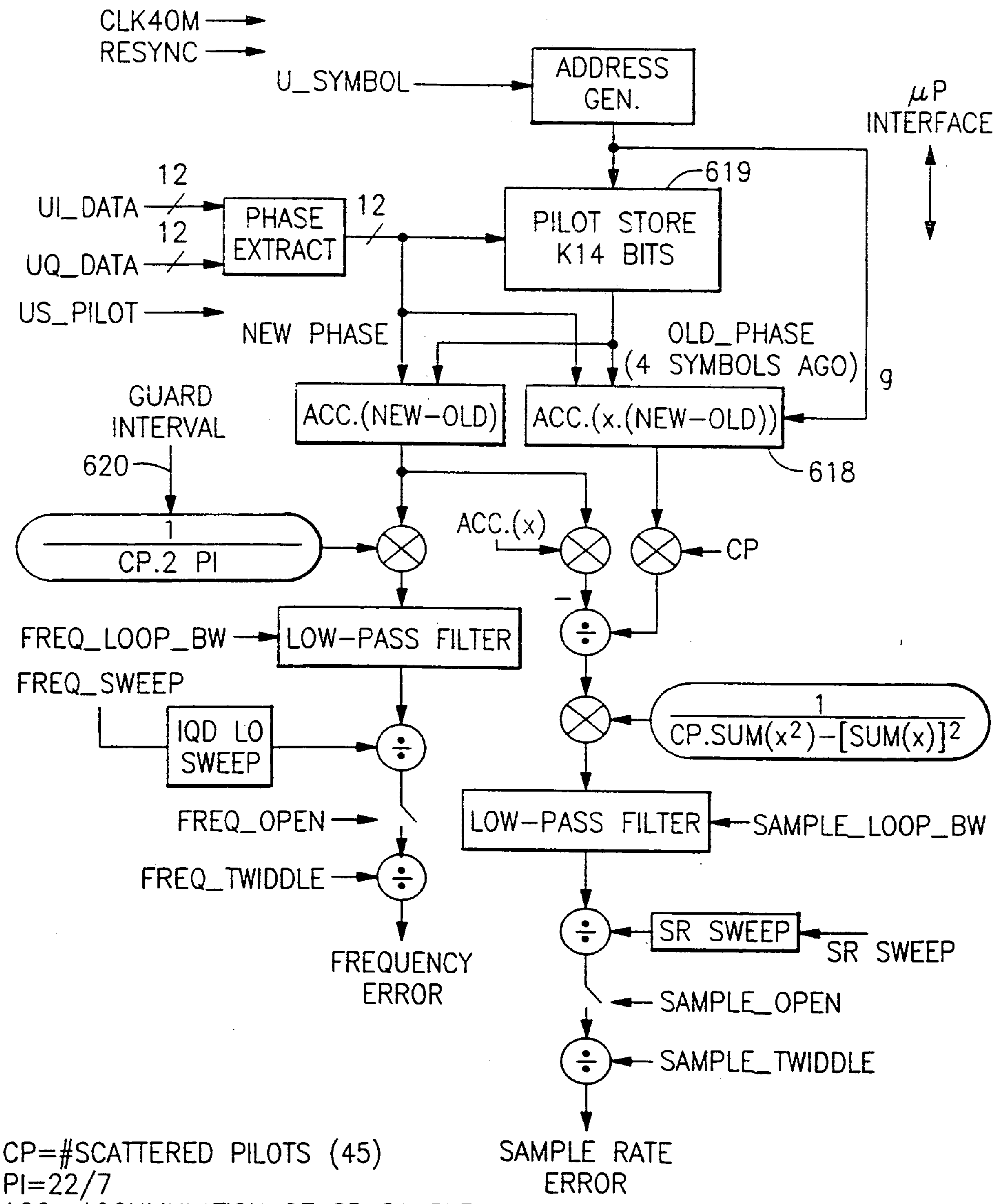

PHASE
604
PHASE DIFFERENCE
PILOT k @ SYMBOL n
MINUS
PILOT k @ SYMBOL n+m
FREQUENCY
SCATTERED PILOT
POSITION

FIG.48



CP=#SCATTERED PILOTS (45)
PI=22/7
ACC.=ACCUMULATION OF SP SAMPLES
Tt=SYMBOL PERIOD (DEPENDS ON GUARD)
m=4(SYMBOLS BEFORE SP "PHASE" REPEATS)

FIG.49

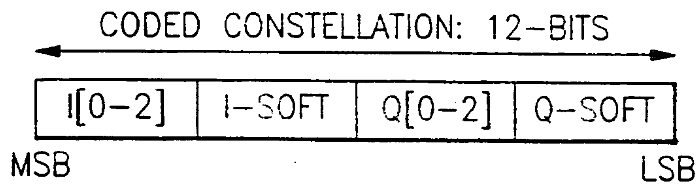

CODED CONSTELLATION: 12-BITS
I[0-2]
I-SOFT
Q[0-2]
Q-SOFT
MSB
LSB

FIG.50

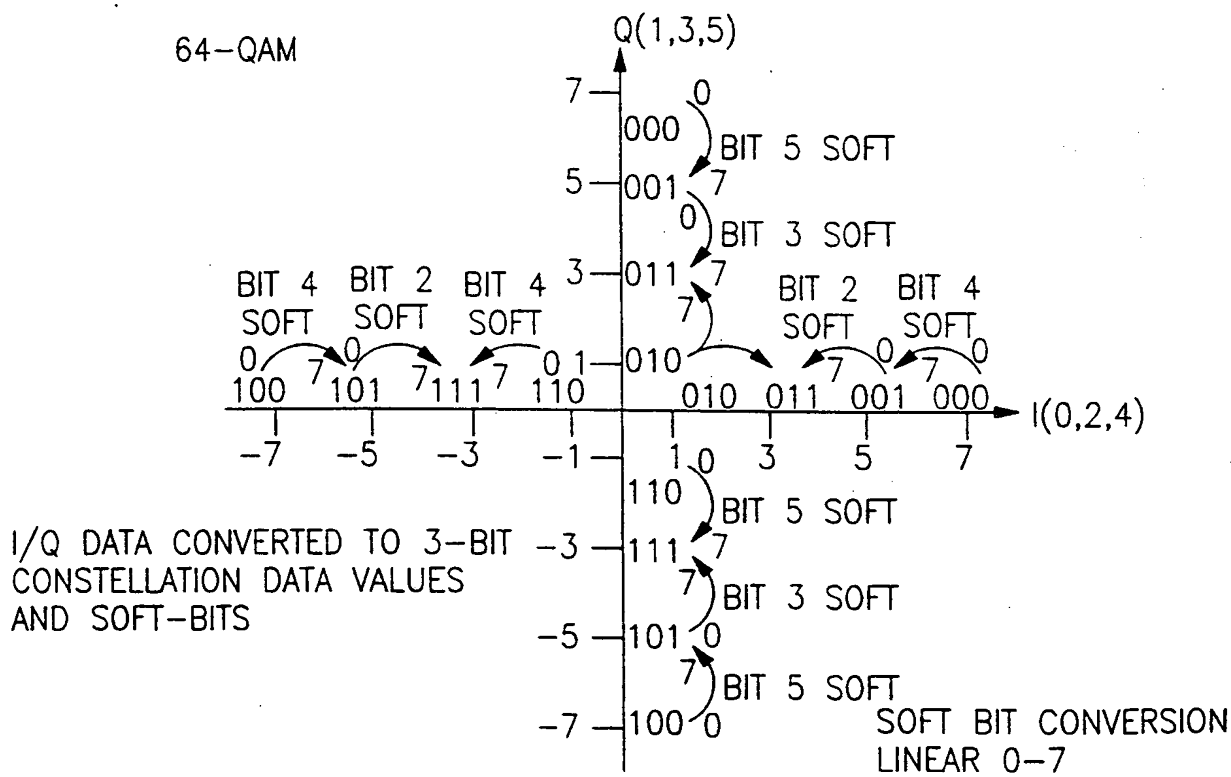

64-QAM
Q(1,3,5)
I(0,2,4)
BIT 5 SOFT
BIT 3 SOFT
BIT 4 SOFT
BIT 2 SOFT
000
001
011
010
110
111
101
100
I/Q DATA CONVERTED TO 3-BIT CONSTELLATION DATA VALUES AND SOFT-BITS
SOFT BIT CONVERSION LINEAR 0-7

FIG.51

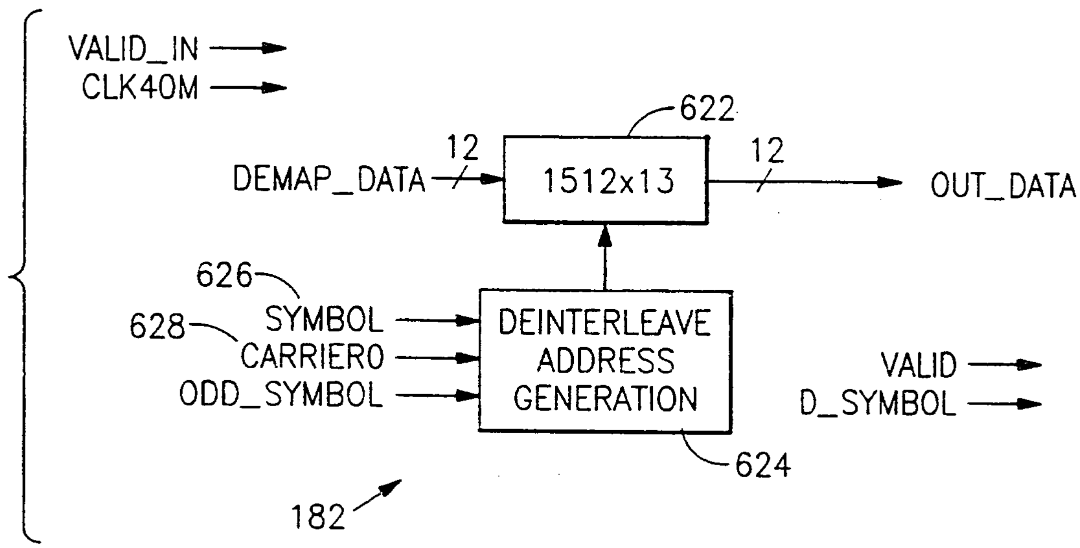

VALID_IN
CLK40M
622
12
DEMAP_DATA
1512x13
12
OUT_DATA
626
SYMBOL
628
CARRIER0
ODD_SYMBOL
DEINTERLEAVE ADDRESS GENERATION
VALID
D_SYMBOL
624
182

FIG.52

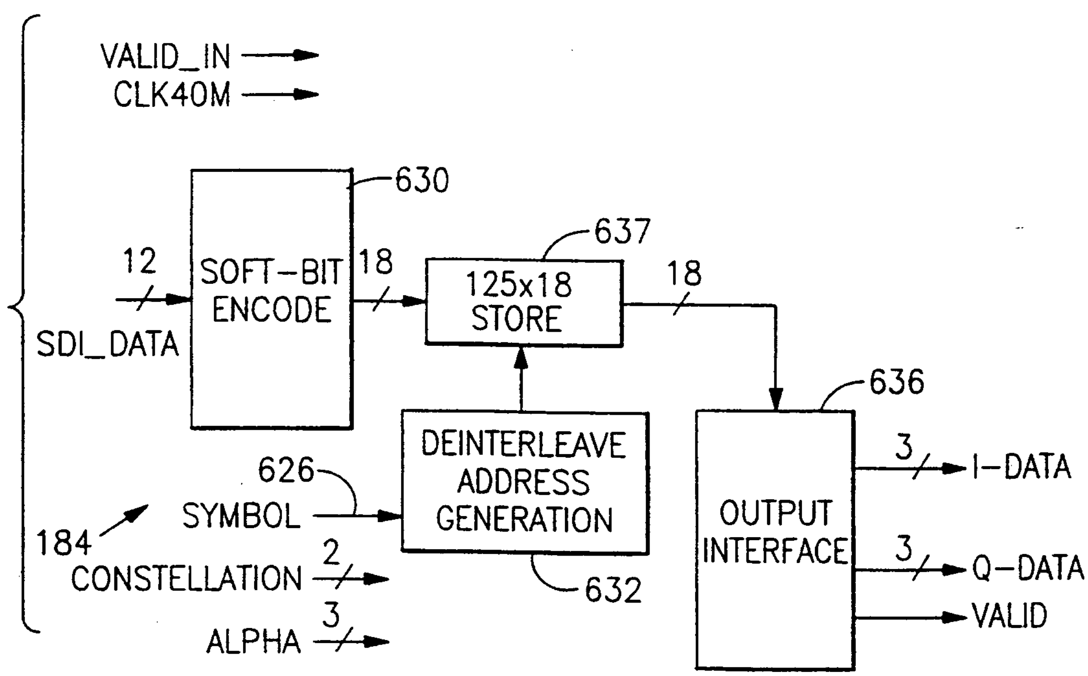

VALID_IN
CLK40M
630
637
12
SOFT-BIT ENCODE
18
125x18 STORE
18
SDI_DATA
636
DEINTERLEAVE ADDRESS GENERATION
626
SYMBOL
3
I-DATA
OUTPUT INTERFACE
184
2
CONSTELLATION
3
Q-DATA
632
3
ALPHA
VALID

FIG.53

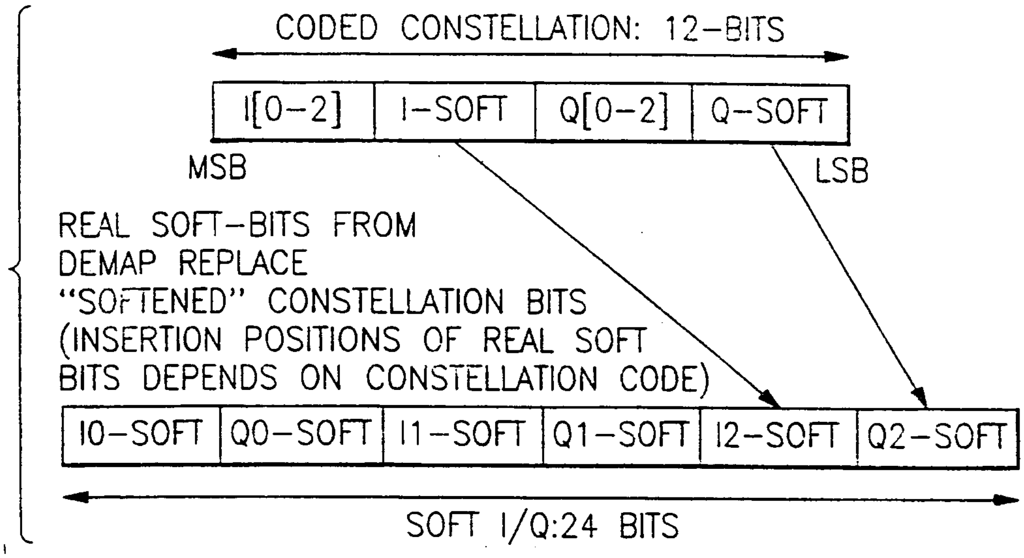

CODED CONSTELLATION: 12-BITS
I[0-2]
I-SOFT
Q[0-2]
Q-SOFT
MSB
LSB
REAL SOFT-BITS FROM DEMAP REPLACE "SOFTENED" CONSTELLATION BITS (INSERTION POSITIONS OF REAL SOFT BITS DEPENDS ON CONSTELLATION CODE)
I0-SOFT
Q0-SOFT
I1-SOFT
Q1-SOFT
I2-SOFT
Q2-SOFT
SOFT I/Q:24 BITS

FIG.54

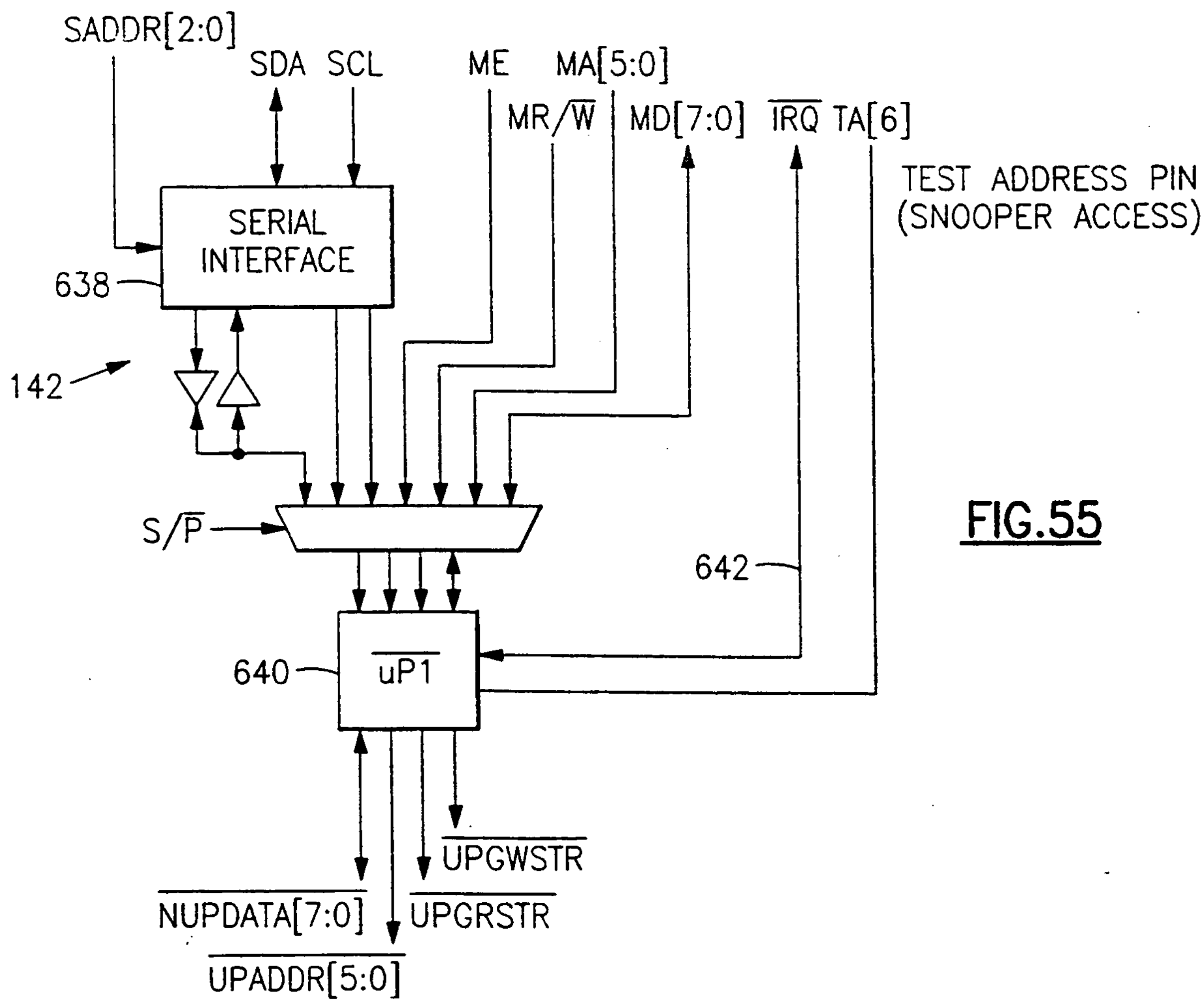

SADDR[2:0]
SDA
SCL
ME
MA[5:0]
MR/$\overline{W}$
MD[7:0]
$\overline{IRQ}$
TA[6]
TEST ADDRESS PIN (SNOOPER ACCESS)
SERIAL INTERFACE
638
142
S/$\overline{P}$
642
640
$\overline{uP1}$
$\overline{UPGWSTR}$
$\overline{NUPDATA[7:0]}$
$\overline{UPGRSTR}$
$\overline{UPADDR[5:0]}$

FIG.55

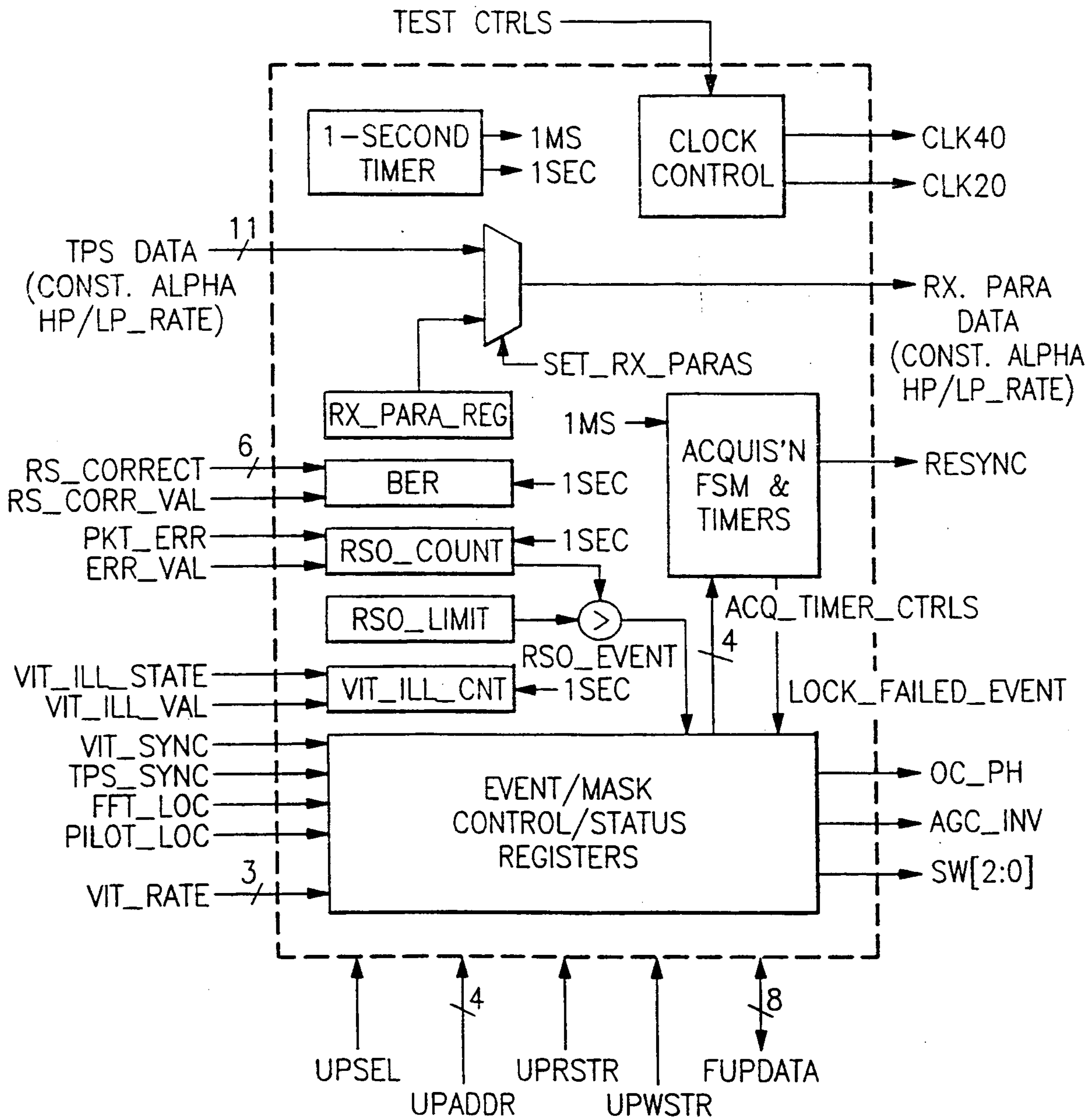

TEST CTRLS
1-SECOND TIMER
1MS
1SEC
CLOCK CONTROL
CLK40
CLK20
11
TPS DATA (CONST. ALPHA HP/LP_RATE)
RX. PARA DATA (CONST. ALPHA HP/LP_RATE)
SET_RX_PARAS
RX_PARA_REG
1MS
ACQUIS'N FSM & TIMERS
RESYNC
6
RS_CORRECT
RS_CORR_VAL
BER
1SEC
PKT_ERR
ERR_VAL
RSO_COUNT
1SEC
RSO_LIMIT
ACQ_TIMER_CTRLS
RSO_EVENT
4
VIT_ILL_STATE
VIT_ILL_VAL
VIT_ILL_CNT
1SEC
LOCK_FAILED_EVENT
VIT_SYNC
TPS_SYNC
FFT_LOC
PILOT_LOC
EVENT/MASK CONTROL/STATUS REGISTERS
OC_PH
AGC_INV
SW[2:0]
3
VIT_RATE
4
8
UPSEL
UPADDR
UPRSTR
UPWSTR
FUPDATA

FIG.56

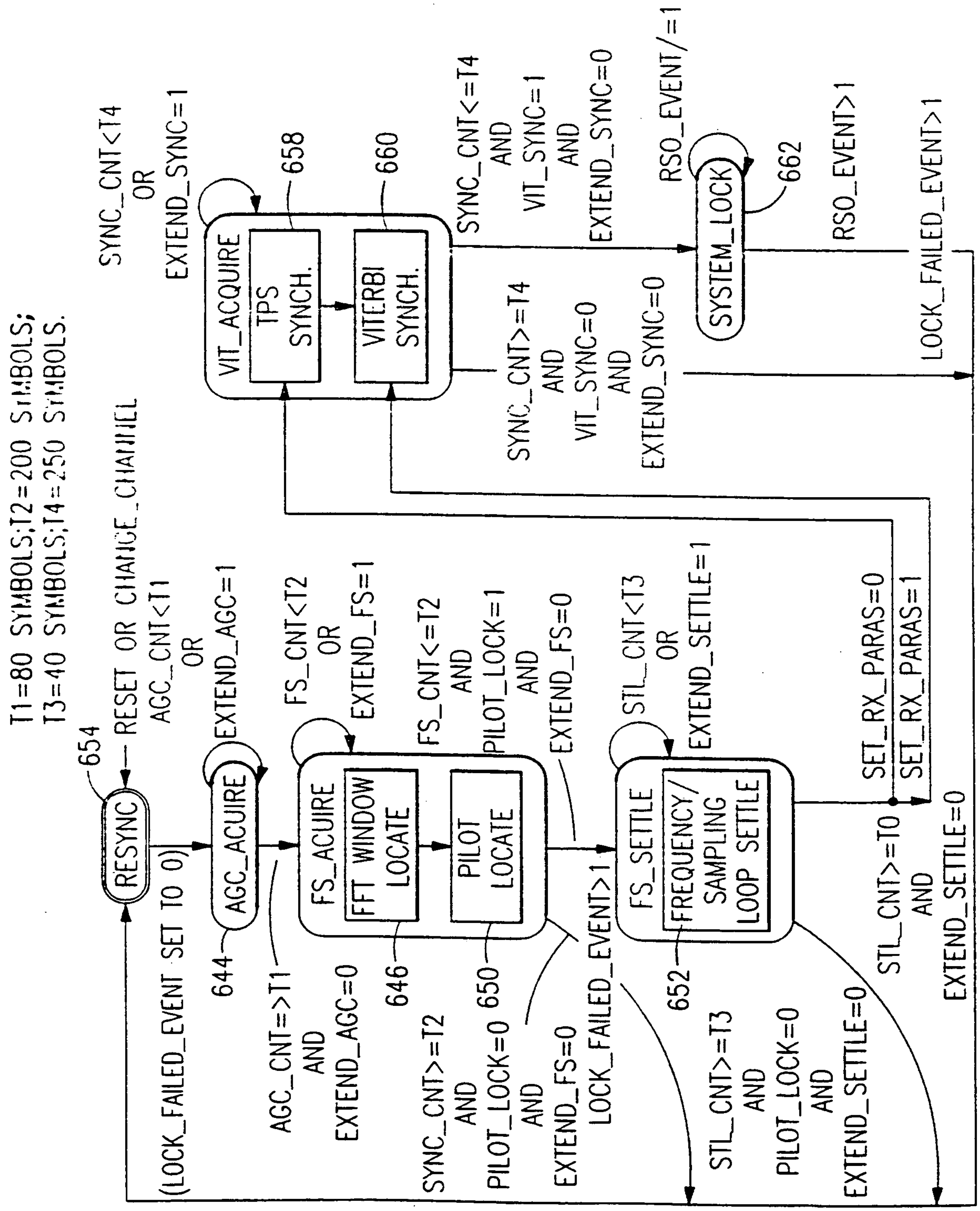

T1=80 SYMBOLS;T2=200 SYMBOLS;
T3=40 SYMBOLS;T4=250 SYMBOLS.
654
RESET OR CHANGE CHANNEL
(LOCK_FAILED_EVENT SET TO 0)
RESYNC
AGC_CNT<T1
OR
EXTEND_AGC=1
AGC_ACUIRE
644
AGC_CNT=>T1
AND
EXTEND_AGC=0
FS_CNT<T2
OR
EXTEND_FS=1
FS_ACUIRE
FFT WINDOW LOCATE
PILOT LOCATE
646
650
FS_CNT<=T2
AND
PILOT_LOCK=1
AND
EXTEND_FS=0
SYNC_CNT>=T2
AND
PILOT_LOCK=0
AND
EXTEND_FS=0
LOCK_FAILED_EVENT>1
STL_CNT<T3
OR
EXTEND_SETTLE=1
FS_SETTLE
FREQUENCY/ SAMPLING LOOP SETTLE
652
STL_CNT>=T3
AND
PILOT_LOCK=0
AND
EXTEND_SETTLE=0
SET_RX_PARAS=0
SET_RX_PARAS=1
STL_CNT>=T0
AND
EXTEND_SETTLE=0
SYNC_CNT<T4
OR
EXTEND_SYNC=1
VIT_ACQUIRE
TPS SYNCH.
VITERBI SYNCH.
658
660
SYNC_CNT<=T4
AND
VIT_SYNC=1
AND
EXTEND_SYNC=0
SYNC_CNT>=T4
AND
VIT_SYNC=0
AND
EXTEND_SYNC=0
RSO_EVENT/=1
SYSTEM_LOCK
662
RSO_EVENT>1
LOCK_FAILED_EVENT>1

FIG.57

PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :
H04L 27/26, G06F 17/14, H04L 1/00 A3

(11) International Publication Number: **WO 98/19410**

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(30) Priority Data:
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9720550.4 26 September 1997 (26.09.97) GB

(71) Applicant: DISCOVISION ASSOCIATES [US/US]; Suite 200, 2355 Main Street, P.O. Box 19616, Irvine, CA 92623 (US).

(72) Inventors: ALAM, Dawood; 15 Westbury Park, Durdham Down, Bristol BS6 7JA (GB). COLLINS, Matthew, James; Flat 1, 4 New King Street, Bath BA1 2BN (GB). DAVIES, David, Huw; 6 Glen Brook, Glen Drive, Stoke Bishop, Bristol BS9 1SB (GB). KEEVILL, Peter, Anthony; 7 Junction Road, Oldfield Park, Bath BA2 3NQ (GB). NOLAN, John, Matthew; 19 The Firs, Combe Down, Bath, Somerset BA2 5ED (GB). FOXCROFT, Thomas; 52B Pembroke Road, Clifton, Bristol BS8 3DT (GB). PARKER, Jonathan; 66 Third Avenue, Oldfield Park, Bath BA2 3NZ (GB).

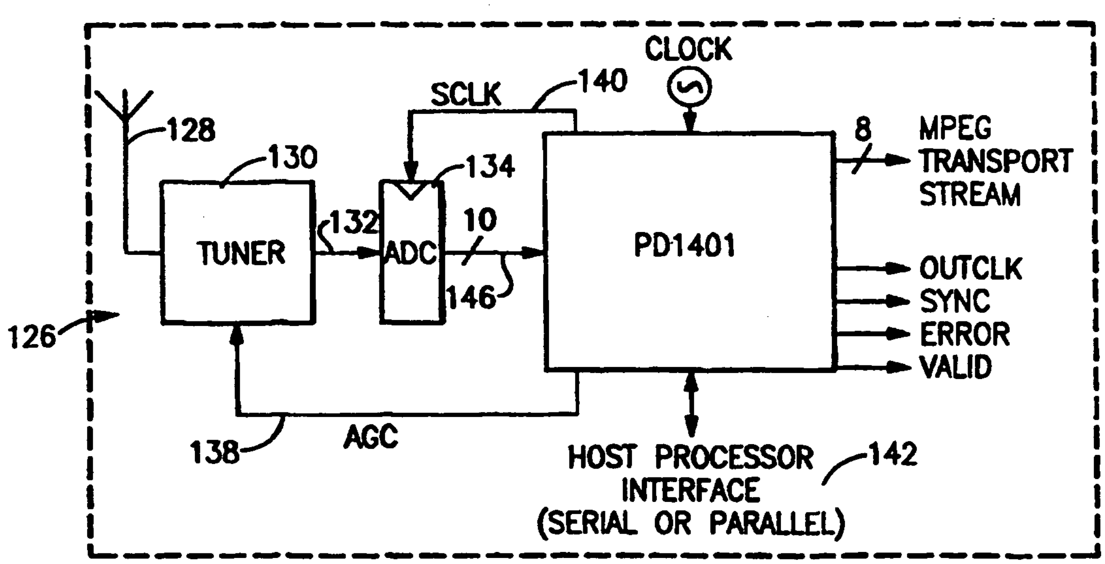
(74) Agent: BICKEL, Arthur, S.; Suite 200, 2355 Main Street, P.O. Box 19616, Irvine, CA 92623 (US).

(81) Designated States: AL, AM, AT, AU, AZ, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, TJ, TM, TR, TT, UA, UG, UZ, VN, ARIPO patent (GH, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(88) Date of publication of the international search report: 27 August 1998 (27.08.98)

(54) Title: SINGLE CHIP VLSI IMPLEMENTATION OF A DIGITAL RECEIVER EMPLOYING ORTHOGONAL FREQUENCY DIVISION MULTIPLEXING



(57) Abstract

The invention provides a single chip implementation of a digital receiver for multicarrier signals that are transmitted by orthogonal frequency division multiplexing. Improved channel estimation and correction circuitry are provided. The receiver has highly accurate sampling rate control and frequecy control circuitry. BCH decoding of tps data carriers is achieved with minimal resources with an arrangement that includes a small Galois field multiplier. An improved FFT window synchronization circuit is coupled to the resampling circuit for locating the boundary of the guard interval transmitted with the active frame of the signal. A real-time pipelined FFT processor is operationally associated with the FFT window synchronization circuit and operates with reduced memory requirements.

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INTERNATIONAL SEARCH REPORT

Inter. nal Application No
PCT/US 97/18911

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04L27/26 G06F17/14 H04L1/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP 0 730 357 A (TELIA AB) 4 September 1996 see abstract see figure 1 see figure 10	1,4
A		2

Y	US 4 300 229 A (HIROSAKI BOTARO) 10 November 1981 see abstract see column 15, line 15 - line 32; figure 4 see column 39, line 59 - line 60	1,4
A		

A	EP 0 653 858 A (TOKYO SHIBAURA ELECTRIC CO) 17 May 1995 see abstract see figure 5	1,2

	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

2

Date of the actual completion of the international search	Date of mailing of the international search report
5 March 1998	07. 07. 98

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Koukourlis, S

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WIRELESS PERSONAL COMMUNICATIONS, vol. 2, no. 4, 1 January 1996, pages 321-334, XP000589621 WYATT-MILLINGTON W ET AL: "A PIPELINED IMPLEMENTATION OF THE WINOGRAD FFT FOR SATELLITE ON-BOARD MULTI-CARRIER DEMODULATION" see page 321, paragraph 2 - paragraph 3	1
A	WO 95 03656 A (TELIA AB ;ISAKSSON MIKAEL (SE); ENGSTROEM BO (SE)) 2 February 1995 see abstract see page 7, line 15 - line 20 see figure 4	1
A	WO 96 24989 A (ADC TELECOMMUNICATIONS INC) 15 August 1996 see page 61, line 26 - page 62, line 6 see page 84, line 4 - page 85, line 9 see figures 11,27	1
A	EP 0 722 235 A (MATSUSHITA ELECTRIC IND CO LTD) 17 July 1996 see figure 2	1
A	EP 0 689 314 A (NOKIA TECHNOLOGY GMBH) 27 December 1995 see figure 2	1

2

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 97/18911

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. [ ] Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. [ ] Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

3. [ ] Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1-4: Receiver for multicarrier signals comprising FFT synchronisation circuit for locating a boundary of the guard interval;
5-7,10-24: functions performed by the FFT processor;
8,9,27-35: channel estimation and correction
25,26: BCH decoder

1. [ ] As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. [ ] As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. [ ] As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. [X] No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1 - 4

Remark on Protest

[ ] The additional search fees were accompanied by the applicant's protest.

[ ] No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 97/18911

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0730357 A	04-09-96	NO 960759 A	02-09-96
		SE 9500743 A	02-09-96
US 4300229 A	10-11-81	JP 1496399 C	16-05-89
		JP 55112054 A	29-08-80
		JP 63046619 B	16-09-88
		JP 1496400 C	16-05-89
		JP 55112055 A	29-08-80
		JP 63046620 B	16-09-88
		JP 1496401 C	16-05-89
		JP 55112056 A	29-08-80
		JP 63046621 B	16-09-88
		JP 1478950 C	10-02-89
		JP 56093449 A	29-07-81
		JP 63026575 B	30-05-88
		AU 527333 B	24-02-83
		AU 5563480 A	28-08-80
		CA 1134519 A	26-10-82
EP 0653858 A	17-05-95	JP 7143097 A	02-06-95
		CA 2135970 A	17-05-95
		US 5602835 A	11-02-97
WO 9503656 A	02-02-95	SE 500986 C	17-10-94
		EP 0712555 A	22-05-96
		SE 9302453 A	17-10-94
		US 5652772 A	29-07-97
WO 9624989 A	15-08-96	AU 4915896 A	27-08-96
		AU 4916296 A	27-08-96
		BR 9607031 A	04-11-97
		CA 2211117 A	15-08-96
		CA 2211803 A	15-08-96
		CZ 9702487 A	17-12-97
		EP 0809898 A	03-12-97
		EP 0808534 A	26-11-97
		FI 973134 A	06-10-97
		WO 9624995 A	15-08-96
EP 0722235 A	17-07-96	CA 2166599 A	11-07-96

International Application No
PCT/US 97/18911

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0722235 A		JP 8251135 A	27-09-96
EP 0689314 A	27-12-95	FI 942876 A	17-12-95